A Prototype Transformer Insulation Condition Monitoring System

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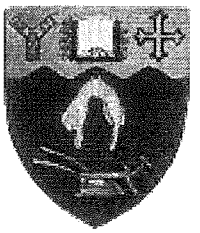

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Dedicated to Lee-Anne Hamilton

Abstract

A prototype data acquisition and processing system is developed for evaluating the insulation condition of a power transformer winding in real-time. The Transformer Insulation Condition Monitoring System (TICMS) evaluates the insulation condition by calculating the winding transadmittance function. The winding transadmittance function is used to fingerprint the insulation system and provides a means of monitoring its condition. The use of a transfer function for evaluating the insulation condition of a power transformer winding was proposed by Malewski and Poulin in 1988 [6, Chapter 1]. The work described in this thesis extends their work in a number of important areas and makes the following contributions to the state-of-the-art. Firstly, the TICMS is able to calculate the transadmittance function to 3MHz, which is sufficient to detect breakdown between individual turns in an Extra High Voltage (EHV) transformer. This is a key distinguishing feature of this work and is important as faults between individual turns can quickly snowball into a catastrophic failure. Previous attempts have been successful at determining the transadmittance function to around 1.5MHz, which only allows breakdown between discs to be detected in an EHV transformer. Second, the TICMS is able to determine the transadmittance function on-line and in real-time for a fully energised transformer. This is another key distinguishing feature of this work as it allows action to be taken to remove a faulty transformer from service prior to catastrophic failure. Previous attempts have calculated the transadmittance function in an offline situation over a period of minutes using pre-recorded data.

Recent advances in analog-to-digital converter (ADC) technology and the availability of high speed Digital Signal Processors (DSPs) have made it possible to extend the work of Malewski and Poulin as described above. This thesis describes the key design features of the TICMS which provide it with the ability to determine the transadmittance function over a 3MHz bandwidth in real-time. These features include the application of an excitation with tailored spectral characteristics, a novel transducer arrangement that allows the effective dynamic range of the digitizer to be extended and at the same time online measurements to be performed, a first-in-first-out (FIFO) memory arrangement that allows the high speed data acquisition section to easily interface to the data processing section, and a powerful 32-bit floating point Digital Signal Processor (DSP) that enables the transadmittance function to be determined in real-time. The graphical user interface to the laboratory prototype is also presented.

Also described are the signal processing techniques, both applied and developed, that are used by the TICMS to determine the transadmittance function in real-time. These include the deconvolution of the voltage and current channel transducer output signals, a radix-2 decimation-in-time (DIT) fast Fourier transform (FFT) algorithm that transforms the voltage and current channel inputs into the frequency domain simultaneously, the calculation of the transadmittance function magnitude and phase from the recorded transients, and a zooming algorithm that is used to accurately determine pole height.

The transadmittance function of a 7.5kVA 11kV/230V distribution transformer is determined and compared with that obtained by performing a time consuming sweep frequency test. Artificial faults are inserted into a 2nd 7.5kVA 11kV/230V distribution transformer to establish relationships between the location and size of a fault and the corresponding changes in the transadmittance function. Sets of tests are conducted to evaluate the effect of fault size, fault location, the introduction of simulated partial discharges, and single turn faults. The ability of the system to detect single turn faults is a key feature as this allows faults to be detected before they can snowball into catastrophic failures.

The effect of temperature on the location and height of poles in the transadmittance function of a 7.5kVA 11kV/220V distribution transformer is established through the use of the TICMS. On-line testing of an energised transformer is performed to evaluate the effect of supply voltage magnitude, load current magnitude, and the point in the 50Hz AC cycle when the insulation test is initiated. This information allows the system to compare successive transadmittance functions and generate an alarm signal if insulation condition degradation is found to have taken place. This information will allow the system to eventually become a 'black box' that permanently sits beside a transformer continuously evaluating insulation condition.

Acknowledgments

I would like to thank my supervisor, Associate Professor Mike Dewe, who through his research efforts in South Africa established a basis for this project. Through his experiences and involvement with the development of other state-of-the-art power system instrumentation systems, I had available resources and development tools that directly benefited the development of my system.

I would also like to thank him for compiling an extensive collection of literature relating to this project while away on study leave in South Africa during 1990. It was a tremendous help and provided this project with a lot of momentum during it's initial stages.

Contents

Glossary of Terms & Abbreviations

ADC - Analog-to-Digital Converter

AF/AE - Almost Full/Almost Empty

ALU - Arithmetic Logic Unit

ANN - Artificial Neural Network

ARAU - Auxiliary Register Arithmetic Units

BIL - Basic Insulation Level

BITE - Build-In Test Equipment

BJT - Bipolar Junction Transistor

bps - bits per second

BW - Bandwidth

CLB - Configurable Logic Block

CMOS - Complementary Metal Oxide Semiconductor

COM Port - Communication Port

CPU - Central Processing Unit

CT - Current Transformer

CTS (active low) - Clear to Send

DAPM - Data Acquisition and Processing Module

DCD - Data Carrier Detect

DCE - Data Communication Equipment

DFT - Discrete Fourier Transform

DGA - Dissolved Gas Analysis

DIP - Dual Inline Package

DIT - Decimation In Time

DMA - Direct Memory Access

DP - Degree of Polymerisation

DPDT - Double Pole Double Throw

DSP - Digital Signal Processor

DSR - Data Set Ready

DTE - Data Terminal Equipment

DTR - Data Terminal Ready

EEE - Electronic and Electrical Engineering

EHV - Extra High Voltage

EIA - Electronic Industries Association

EM - Electromagnetic

EMI - Electromagnetic Interference

ENOB - Effective number of bits

EOL - End of Life

EPROM - Erasable Programmable Read-Only Memory

ESL - Equivalent Series Inductance

ESR - Equivalent Series Resistance

FF - Flip-Flop

FFA - Furfuraldehyde

FFT - Fast Fourier Transform

FIFO - First In First Out

FIR - Finite Impulse Response

FPGA - Field Programmable Gate Array

FRA - Frequency Response Analysis

FRSL - Frequency Response of Stray Losses

GUI - Graphical User Interface

HDD - Hard disk drive

HiZ - High Impedance

HPLC - High Performance Liquid Chromatography

HV - High Voltage

IACK - Interrupt Acknowledge

IC - Integrated Circuit

IDFT - Inverse Discrete Fourier Transform

IEEE - Institute of Electrical and Electronics Engineers

IFFT - Inverse Fast Fourier Transform

IGM - Impulse Generator Module

I/O - Input/Output

IOB - Input/Output Block

ISR - Interrupt Service Routine

IVT - Interrupt Vector Table

KCL - Kirchoffs Current Law

KVL - Kirchoffs Voltage Law

LCD - Liquid Crystal Display

LED - Light Emitting Diode

LSB - Least Significant Bit

LV - Low Voltage

LVI - Low Voltage Impulse

MDI - Multiple Document Interface

MFLOPS - Million Floating Point Operations Per Second

MODEM - Modulator/Demodulator

MSB - Most Significant Bit

MUX - Multiplexer

NPG - Negative edge Pulse Generator

PC - Personal Computer

PCB - Printed Circuit Board

PD - Partial Discharge

PLCC - Plastic Leaded Chip Carrier

PPG - Positive edge Pulse Generator

PPR - Partitioning Placing and Routing

PROM - Programmable Read Only Memory

QFP - Quad Flat Pack

RAM - Random Access Memory

RDCLK - Read Clock

RI - Ring Indicator

RS-232 - Recommended Standard 232

RTD - Resistance Temperature Device

RTS (active low) - Request to Send

RxRDY - Receiver Ready

SCP - Serial Configuration PROM

SDU - Serial Data Unit

SIN - Serial input

SINAD - Signal to Noise and Distortion Ratio

SNR - Signal to Noise Ratio

SOUT - Serial output

SRAM - Static Random Access Memory

TCG - Total Combustible Gas

TD - Transient Digitiser

TDRPG - Transient Digitiser Reset Pulse Generator

TI - Texas Instruments

TICMS - Transformer Insulation Condition Monitoring System

TSM - Test Synchroniser Module

TUT - Transformer Under Test

UART - Universal Asynchronous Receiver Transmitter

UV - Ultra Violet

UHV - Ultra High Voltage

μP – Microprocessor

WRTCLK - Write Clock

Chapter 1

INTRODUCTION

The increasing complexity of electrical supply networks, including the use of reactive compensation equipment and the effects of consumer loads, has led to undesirable harmonic pollution and transient signals being fed into the network. These effects, together with lightning impulses and other abnormal situations following network fault conditions, have placed additional burdens on the insulation systems of high voltage power equipment.

Large transformers form a critical part of any power system. Their reliable and continued operation is the key to profitable generation and transmission. Their costs of acquisition, replacement, transportation, installation and repairs are among the highest in a system. Their failures create losses of revenues and are problematic for the following reasons:

- Generally large power transformers are situated so that failures present operational problems to the system.
- Large power transformers are encased in tanks of flammable and environmentally hazardous fluid and failures are often accompanied by fire and/or spillage of this fluid.
- Transformer replacement involves high capital cost and may be affected by long manufacturing lead time for larger transformers.
- Catastrophic failures can generate substantial costs in terms of peripheral equipment destruction and loss of revenue through service outages.
- Explosions that result from catastrophic failure can endanger the lives of nearby personnel.
- Failures lead to unplanned emergency utilization of resources.

Consequently there has been a definite trend in utility organisations to take greater interest in the condition of high voltage power equipment on their networks. Although periodic monitoring of equipment and proper maintenance activities will prevent a large proportion of failures in service, a combination of older equipment and undesirable overvoltages and harmonics has shown that periodic monitoring will not always identify a potential failure.

The following motivations provide further reasons for utilities to take a greater interest in the insulation condition of transformers in their networks:

- Transformer loading has a major effect on it's insulation stresses and as a result insulation systems are designed to satisfy the in-service performance requirements. In most cases electrical equipment is operated well within its design limits and under normal steady state operating conditions the electrical and thermal stresses on the insulation materials are within their capabilities. However increasing emphasis is being placed on raising the loading of a transformer beyond it's nameplate rating due to system expansion. The resulting thermal and electrical stresses affect the service life of the insulation [4].
- The cost of replacing an old transformer which may or may not be at the end of its life, makes it worthwhile to assess whether it's life can be extended on the basis of it's present condition or by refurbishing at a convenient point in time.
- With advancements in the knowledge of the performance of old and new insulating materials and the highly competitive manufacturer's environment, new transformers are being designed and built to very much tighter design tolerances and safety margins [2].
- The levels and frequency of electrical stresses that transformers are being subjected to is continually increasing as a result of the increased use of fast solid-state power switching equipment by consumers [2].
- The normal quiescent state of a transformer does not draw attention to incipient faults which may develop from a gradual deterioration of its insulation. These faults may be detected during routine maintenance, but the ability to have detailed information on the state of health of a transformer prior to carrying out maintenance work or alterations becomes a significant asset and adds an element of preventative maintenance to the operation of transformers.

1.1 Existing Techniques

Transformer insulation condition tends to degrade over tens of years. The degradation can be attributed to aging, high operating temperatures, transient voltages etc. At present the most often employed method for determining the insulation condition is to take oil samples from the tank at periodic intervals. These oil samples are then taken off for analysis in order to determine what dissolved constituents are present as this gives an indication of insulation condition. On the basis of the results of these tests the transformer may be taken out of service for maintenance. Because oil sampling only happens on a periodic basis, e.g. a well setup system may take oil samples every 6 weeks, then often insulation condition

degradation can be missed. Furthermore, depending on whether the transformer has been in service immediately prior to the oil samples being taken or not, the actual oil samples taken may not give a true picture of the state of the oil throughout the transformer tank (i.e. it may give misleading information on the state of the insulation). Consequently there have been a large number of power transformer failures, especially on EHV systems.

Over recent years investigations into other diagnostic techniques for determining the condition of transformer insulation have been many and varied. Other techniques include DGA, TCG, furanic compound analysis using HPLC, analysis of DP measurements, analysis of tank pressure measurements, dielectric response testing, LVI testing, analysis of leakage inductance measurements, FRA, partial discharge detection, and analysis of thermal measurements. However operating utilities around the world are still experiencing sudden, unexpected and occasionally catastrophic failures. Clearly new technology or more efficient and effective use of existing technology is needed to prevent such failures.

Advances in electronic and computer instrumentation and measurement technology have made the application of microprocessor/DSP based surveillance systems a reality. Systems are available that monitor substation equipment, providing automatic control features and information to network control centers. Although the sensors required are generally expensive items, microprocessors are relatively cheap compared to other recording devices and can manage a larger number of inputs. Furthermore, the microprocessor outputs can be arranged to provide system operators with the necessary information to take action or else can be linked directly to the control and protection systems to provide automatic disconnection of suspect units before failure.

1.2 The Transadmittance Function Method

A new method for evaluating the insulation condition of a power transformer winding has been proposed by Malewski and Poulin [6]. The technique consists of determining the winding transadmittance function in the frequency domain, by deconvolution using the applied impulse voltage and neutral current recorded during an impulse test. The transadmittance function is characteristic of the winding under test and in theory is independent of the form of the applied impulse. The integrity of the winding is determined by comparing the transadmittance functions obtained at full and reduced test voltage levels. Differences between the transadmittance functions reveal local breakdowns in the winding that can be dissociated from partial discharges. Malewski and Poulin claim that the method permits unambiguous acceptance or rejection of a transformer.

A transformer in general possesses a limited number of major resonances which are determined by the winding construction. Three main types of winding are used in transformers, namely disc, interleaved disc, and layer. Disc and sometimes interleaved disc windings are used for the primary winding of EHV transformers. Over a frequency range of 20kHz to 1.2MHz, disc windings have a dominant pole around 0.5-0.6MHz, interleaved disc have a few major poles between 0.3 and 0.8MHz while layer windings show a number of overlapping adjacent poles [7][8]. Breakdown between adjacent turns in an EHV transformer usually excites an oscillation at approximately 2.5MHz [6]. Malewski and Poulin were able to determine the winding transadmittance function to 1MHz and therefore were unable to detect breakdown between individual turns in a winding. Further because the system took approximately 4 minutes to complete the comparison of two transadmittance functions, online real-time insulation condition monitoring was not possible.

This project involves the development of a prototype DSP based instrumentation system that can determine the winding transadmittance function to 3MHz in real-time (less than 100ms). The Transformer Insulation Condition Monitoring System (TICMS) hardware design (discussed in Chapter 4) and signal processing techniques (Chapter 5) allow the transadmittance function bandwidth to be extended to 3MHz, allowing the detection of faults between individual turns in a winding. The system has been interfaced to an energised transformer and used to determine the transadmittance function in real-time. Real-time monitoring will allow the system to activate an alarm, notifying substation personnel that a failure may take place.

1.3 The TICMS

The different components making up the TICMS are shown in Figure 1.1 and are described below.

- **Impulse Generator Module (IGM):** This supplies the excitation needed to determine the transadmittance function of the transformer under test. The IGM produces a low voltage impulse and can be activated either manually or by the DAPM under software control. The IGM is discussed in further detail in 4.2.
- **Transducers:** Transducers are used on the voltage and current channels to transform the test signals into a form compatible with the DAPM design. The characteristics of each transducer enable the system to be used on-line without interfering with the in-service operation of the transformer. Further details on the transducers are given in 4.4.
- **Data Acquisition and Processing Module (DAPM):** The DAPM is the heart of the

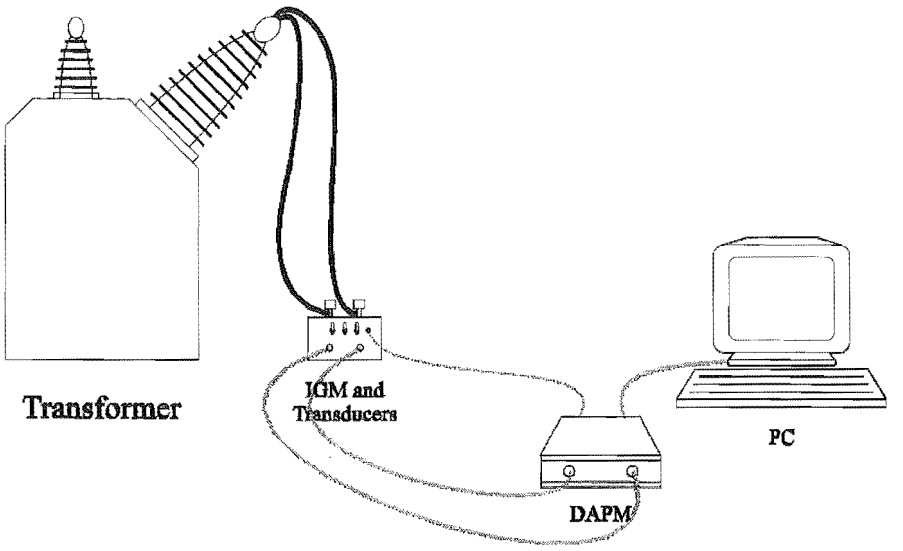

Figure 1.1 The Transformer Insulation Condition Monitoring System

TICMS. The DAPM digitises the supplied excitation and the resulting transformer response and performs the digital signal processing operations required to determine the transadmittance function. By using a 32-bit floating point DSP, the DAPM is able to determine the transadmittance function in real-time. The DAPM is discussed in further detail in 4.6

- **PC:** An attached PC provides a user interface to the DAPM. Through the use of customed designed Windows95 software, the PC can receive and display test data in a variety of graphical formats. The PC application software can save unprocessed DAPM data into a text file, allowing the data to be imported into MATLAB so that existing DSP algorithms can be refined and new ones developed, leading to a reduction in development time. The PC application software controls the operation and configuration of the DAPM by sending commands words over the serial link connecting the two. The software is discussed in greater depth in 6.4.

Ultimately the decision on whether or not to introduce such technology must be an economic one in which the cost of its introduction must be outweighed by the losses incurred through failures, outages and inefficient maintenance procedures. As time progresses so the relative cost of applying high technology decreases and in the opinion of the author, it is only a matter of time before the introduction of sophisticated condition monitoring equipment becomes widespread.

1.4 Thesis Overview

The contents of this thesis consists of the following main components

- A review of existing diagnostic and monitoring techniques
- The hardware, signal processing and software design of the TICMS
- Using the TICMS to perform both offline and online testing on 7.5kVA 11kv/220V single phase distribution transformers

These components are discussed in the following chapters

- **Chapter 2:** The purpose of this chapter is to present background information on existing fault detection and diagnostic techniques and to identify the shortcomings and limitations of each.
- **Chapter 3:** This chapter reviews trends and recent developments in on-line condition monitoring of power, distribution and instrument transformers. Monitoring systems based on temperature measurements, differential relays, transformer modeling, partial discharge detection, dissolved gas analysis, and other methods are discussed and some currently available monitoring equipment is described. Discussions on the presented techniques include existing systems and practices along with their capabilities and success rates. Because the assessment of the remaining life of a transformer is one of the most important issues related to monitoring, a section on transformer life assessment is presented. Sections on transformer impulse testing and the transfer function method have been included as this material directly relates to the transformer insulation condition monitoring system developed by the author.
- **Chapter 4:** The purpose of this chapter is to describe the hardware design of the TICMS prototype. The first section gives an overview of the design and identifies the main modules. Section two describes the impulse generator module (IGM) used to excite the transformer while section three presents the design of the transducers used to interface the transformer to the data acquisition and processing module (DAPM). The buffers and transmission lines used to connect the IGM to the DAPM are discussed in section four while the design of the DAPM and each of its components are presented in the remaining sections.
- **Chapter 5:** The purpose of this chapter is to describe the signal processing principles used in the design of the TICMS and the application of those principles to the problem of determining the transadmittance function to 3MHz with sufficient accuracy. In the first section a general overview of the signal processing system along with its requirements is presented. The second section describes the sampling and quantisation operations that take place during data acquisition and discusses the influence of these operations on the TICMS design. Next the design of the transducers employed in the TICMS and their intentional affect on the signals being acquired is described. The

following sections present some underlying Fourier theory needed to understand subsequent TICMS signal processing operations. These include the computationally efficient FFT algorithm used in the TICMS design and the signal processing operations needed to determine the transadmittance function magnitude and phase from the acquired signals. The final two sections discuss the application of signal averaging and zooming techniques that are optionally applied in order improve the accuracy of the calculated transadmittance function.

- **Chapter 6:** The purpose of this chapter is to describe the three software designs that have been developed for the TICMS prototype. In the first section the three software designs are introduced and an overview of the software design process used is given. The second section describes in more detail the steps involved in the development of the DAPM application software while the remaining two sections give a functional overview of the TICMS Windows application software and the DAPM diagnostic software.
- **Chapter 7:** The purpose of this chapter is to present the TICMS results from a series of tests designed to evaluate the effect of known faults and operating conditions on the transadmittance function of a single phase 7.5kVA distribution transformer. The first section presents reference transadmittance functions that are used as a basis for comparison in subsequent sections and describes the characteristics of transadmittance function poles that are monitored for change. Subsequent sections present the results of test sets designed to evaluate the effects of artificial faults, transformer internal temperature changes, and core magnetization on the transadmittance function.
- **Chapter 8:** This chapter presents an overview of what has been accomplished, pulls together the main features of previous chapters, and highlights the key contributions made by this thesis to the state-of-the-art in power transformer insulation condition monitoring. Future research and development along with potential directions for the authors work to evolve towards are discussed.

1.5 Aim of the Project

The aim of this project has been to initiate, a transformer insulation condition monitoring research program based on the transadmittance function method. This has been performed by developing a prototype DSP based instrumentation system capable of performing on-line measurements and calculations in real-time. The system has been evaluated by testing 7.5kVA distribution transformers.

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Chapter 2

FAULT DETECTION AND DIAGNOSTIC TECHNIQUES

The purpose of this chapter is to present background information on existing fault detection and diagnostic techniques and to identify the shortcomings and limitations of each.

In the present context it is useful to differentiate between "Monitoring" and "Diagnosis". "Monitoring" is here defined as on-line collection of data and includes sensor development and measurement techniques for on-line applications and data acquisition. "Diagnosis" includes interpretation of data and off-line measurements on transformers. Diagnosis and fault detection techniques are discussed in this chapter while monitoring is considered in Chapter 3.

2.1 Transformer Insulation

Insulation is recognized as one of the most important constructional elements of a transformer. Its chief function is to confine the current to useful paths, preventing its flow into harmful channels. Any weakness of insulation may result in failure of the transformer. Since the invention of the power transformer, the conventional conductor insulation has been some form of paper or cloth. The main constituent of these fibrous materials is cellulose, an organic compound whose molecule is made up of a long chain of glucose rings or monomers, typically numbering in the range from 1000-1400 [26][27]. The chemical structure of a portion of a cellulose molecule is shown in Figure 2.1.

In solid insulation systems it is essential to eliminate air or gas from within insulation layers. It is thus necessary to impregnate solid insulation systems such as paper for transformers with suitable oil of adequate dielectric constant to prevent the voltage stresses in the air voids from causing partial discharges and subsequently breakdown. The most commonly used insulating liquid is mineral oil. This is due to the low cost and its ready availability. The alternatives are usually synthetic oils which are used when special

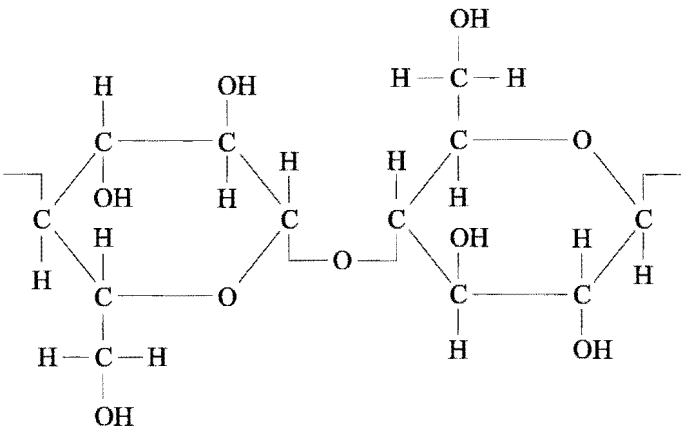

Figure 2.1 Cellulose molecule structure

properties are required. These properties are fire resistance, high permittivity and gas absorbing characteristics. In general though, the combination of mineral oil and cellulose has remained the standard transformer insulation system up to the present time. However newer materials having a higher temperature capability have come into use in the last 25 years [9]. This allows a transformers output to be increased (for a given size and weight) if the allowable average winding temperature can be increased.

Generally an insulating oil serves two primary functions in the transformer, namely cooling and dielectric. To serve as a dielectric medium the oil must be free from water and suspended matter. To act as a cooling medium, an oil requires low viscosity and volatility plus a good heat transfer capability. Additionally the oil must have good oxidation stability. Oxidation will produce oil decay products which cause transformer overheating and premature failure [2].

The electrical quality of the cellulostic material is highly dependent on it's moisture content. When exposed to air, cellulose absorbs moisture from the air quite rapidly. If not impregnated with oil, equilibrium with the moisture content of air is reached in a relatively short time. Thus, cellulostic material has to be processed under heat and vacuum to remove the moisture before oil impregnation in order to obtain maximum dielectric strength. For most applications, a maximum initial moisture content of 0.5% moisture per dry weight cellulose is considered acceptable. For modern EHV and UHV transformers, a maximum initial moisture content of 0.3% or less is recommended [9]. The introduction of moisture in the field during installation and maintenance operations can be problematic [10].

Cellulostic material shrinks when moisture is removed. It also compresses when subjected to pressure. Therefore it is necessary to dry and dimensionally stabilize windings before adjusting them to the desired size during the transformer assembly process. Ideally, the prestabilizing pressure should be equal to or larger than the anticipated loading the winding

will experience during fault conditions, so that further compression of insulation and loosening of windings in service is minimized.

2.1.1 Insulation Aging

Electrical, thermal, mechanical, and environmental stresses are factors attributed to insulation aging. Some of these stresses are prevalent in specific applications. Sometimes these stresses combine into a 'multistress' situation, causing the aging process to accelerate further. One of the most frequently encountered situations in real applications are electrical and thermal stresses, acting simultaneously [11].

Electrical aging takes place when the electrical stresses in an insulation system cause ionisation and partial discharges to occur at operating voltages. Partial discharges should not occur at operating voltages but overvoltages can produce partial discharges which do not disappear at the normal voltage. Environmental effects such as humidity, pressure changes, dust, chemical fumes etc. will contribute to the early onset of partial discharge activity. It is thus important to eliminate these effects particularly when the equipment is operating in harsh environments [8].

Although transformer insulation is affected by many factors, temperature is probably the most severe of the aging factors. The rate of thermal aging of cellulose accelerates rapidly at temperatures not far above the accepted normal operating temperature of transformer conductors. As a result there is an inter-relationship between the life expectancy and the operating temperature of a transformer. A law describing this relationship was put forward by Montsinger in 1930 and in general terms states that an increase or decrease in the operating temperature of 6-10°C, depending on the insulation material, will result in a doubling or halving of the aging rate of the insulation. In 1948, Dakin [12] proposed a theory for the interpretation of thermal aging based on the Arrhenius relationship. This theory, describing the dependence of chemical reaction rates on the temperature, is still used today as a basis of thermal aging [13]. It is given by

$$L = Ae^{B/T} \tag{2.1}$$

where L is the life, T is the temperature, and A, B are constants determined by the activation energy of the reaction. Normal transformer insulation life expectancy is based on a continuous hot spot temperature of 110°C. However hot spot temperatures of 130°C to 140°C are commonly accepted under emergency loading conditions. Relative to 110°C, the aging rate at 130°C accelerates by a factor of 8 and at 140°C by a factor of 21 [9], according to the Arrhenius relationship.

The insulation system of a transformer is invariably stressed to some extent by mechanical forces occurring during the operation of the equipment e.g. forces resulting from short circuit currents. Mechanical stresses can also be a major consideration during the manufacturing and processing stages of production. Residual mechanical stresses will obviously impact on the life of the insulation system in service.

2.2 Existing Maintenance Procedures

Preventative maintenance techniques play an important role in maintaining the heath of transformers. When properly applied they allow early detection of developing faults, allowing steps to be taken to prevent further deterioration and possible subsequent failure. Currently practiced preventative maintenance procedures used to increase transformer insulation reliability include [3]:

- **Visual Inspections:** Defects, abnormalities and the general condition of the transformer are noted together with information on parameters such as oil levels, temperatures, pressures, loadings etc. This is often performed on a scheduled basis and the collected data is evaluated so that decisions on when to request further maintenance can be made.
- **Insulation Resistance Measurements:** Insulation resistance measurements are often made with a Megger during transformer overhauls and repair work and are therefore done on an irregular basis. Because most insulating materials have a very high resistivity, high insulation resistance values are subject to error unless correct procedures are followed.
- **Dielectric Loss Measurement:** Insulation dielectric loss is determined through tanδ measurements. A change in the tanδ during the life of a transformer is a good indication of insulation deterioration. Like insulation resistance tests, tanδ tests are usually made during overhauls and repair work on an infrequent basis.
- **Scheduled examination:** Where transformers are taken out of service and undergo detailed examination. However often transformers which are in good order and have only been subjected to minimal operational stresses are pulled out of service to be dismantled just because they are due. Proposals have been made to relate the service frequency to parameters such as oil temperature(s) and the load integrated with respect to time value [3].
- **Oil analysis:** Where oil samples are taken from the tank at periodic intervals for use in gas chromatography tests in a laboratory. Often a database of results is built up and maintained for each individual transformer. Oil samples are typically taken frequently during a transformers first six months of service but are then only taken once or twice

per annum. Oil analysis techniques are further discussed in 2.3.2. Portable gas chromatography equipment allows testing to be done in the field and on-line as discussed in 3.3.7.

2.3 Diagnosis Overview

Diagnosis is normally used either for determining the actual condition of a transformer, or as a response to a received warning signal. Since it is not a permanent installation, the use of high tech, sophisticated and costly equipment combined with skilled personnel can be justified. The monitoring equipment discussed in Chapter 3 is needed for getting the relevant data, but without well developed methods for interpreting this data and for giving recommendations, there is limited practical value in installing such equipment. It is thus important that diagnostic techniques are used which match the sensor systems installed on transformers. In general, as the diagnostic methods become more advanced, the importance of a deep knowledge of transformer design increases. In many cases, it is not possible to make a reliable diagnosis without knowing the transformer design in detail.

Faults of the HV insulation of power transformers in service can generally be divided into the following three categories, according to the time of evolution [5]:

- An internal discharge caused by a winding displacement following a short circuit current, or a discharge due to a large steep-fronted transient overvoltage may lead to instantaneous and complete breakdown
- Local faults which develop into a complete breakdown over a few days, weeks or even months. These are common and their early detection is the main task of automatic diagnostic devices continuously monitoring transformers in service.
- Long term deterioration of HV insulation (which can be perceived as accelerated aging) over a period of a few years can theoretically be detected by analysing oil samples, usually taken at six or twelve month intervals.

The major stresses acting on the windings of a power transformer, either in combination or individually, are [4]:

- **Mechanical stresses** between conductors, leads and windings due to overcurrents and fault currents caused by system short circuits.
- **Thermal stresses**, due to local overheating, cooling system malfunctions and overload currents and leakage flux when loading above the nameplate rating.
- **Dielectric stresses**, due to system overvoltages, transient impulse conditions and

internal winding resonance within a winding.

Because the monitoring and diagnostic techniques presented in this chapter and the next, are in general sensitive to all three fundamental stresses, then interpretation of the outputs for fault diagnosis can be problematic. Therefore decisions made on the basis of the results of only one diagnostic technique can be misleading. For this reason the final decision regarding insulation failure mechanisms is best made by evaluating and interpreting the results of more than one technique and must take into account the construction characteristics specific to the transformer being tested. A review of currently practiced diagnostic techniques is now presented.

2.3.1 Oil Dielectric Strength Test

The Dielectric Strength Test is performed according to the IEC-156 standard. The dielectric strength of oil, which is effectively a measure of the oil's ability to withstand electrical stress without failure, is exceptionally sensitive to contaminants such as water, sediment and conducting particles. Although combinations of these tend to reduce the dielectric strength of the oil, a high dielectric strength does not necessarily indicate a total absence of contaminants, but simply that the level of contaminants between the electrodes is insufficient to affect the average breakdown voltage of the oil. In performing this test it is important that a sample is taken that has a homogenous distribution of oil impurities without any air bubbles.

The basic test consists of applying to the electrodes an increasing AC voltage at mains frequency, starting from 0V and increasing at steady rate of 2kV/s until the value producing breakdown is reached. Breakdown is then defined as the voltage when the first spark-over occurs, whether transient or established. The test is repeated six times on the same sample. Maximum and minimum times between tests are specified for each test sample. The final result is the arithmetic mean of all six tests. By determining the dielectric strength along with moisture content, loss angle and resistivity etc., an overall assessment of the status of the insulation oil can be made.

2.3.2 Oil Analysis

Oil analysis is one of the primary means used to monitor the insulation condition of power transformers. The frequency at which oil samples are taken is typically as follows:

- Once a month for the first six months of service
- Once or twice annually after the first six months

- Within 24 hours of a fault as a matter of procedure
- Up to once a week for a troublesome transformer

When oil is taken from a transformer for analysis and not replaced the pressure drops slightly. If a large number of such samples are taken over a period of time the pressure may drop to the extent that, in cool weather, negative pressure exists at the top. This condition must be avoided as it encourages contamination with air and moisture. Gases collected by fitted Buchholz relays are also analysed. A discussion of DGA, TCG, and furfuraldehyde oil analysis techniques follows.

2.3.2.1 Dissolved Gas Analysis (DGA)

The presence of faults such as arcing, local overheating and partial discharges in transformers always results in chemical decomposition of the insulating materials, mineral oil and cellulose. The gases formed tend to dissolve, either entirely or partially, in the mineral oil. By monitoring the concentration of these gases, it is possible to detect incipient faults at an early stage and take corrective actions before they lead to unexpected failure.

The laboratory technique used to separate and analyse fault gases is called Dissolved Gas Analysis and is commonly referred to as DGA. The analytical instrument used is a gas chromatograph. The process requires the careful collection of an oil sample which is usually sent to a third party laboratory specializing in transformer oil analysis. The gases are extracted under a vacuum and analysed individually for gas concentration in parts per million (ppm) and percentage.

DGA is often performed in the following situations:

- During a heat run test in a factory
- A few days after a new transformer goes into service
- For routine annual testing as part of a maintenance program
- After a Buchholz alarm or trip during normal operation
- After a protection trip due to a system fault close to the transformer
- After a short circuit condition due to failure of other equipment
- When overheating is suspected due to overloaded operating conditions

The nature and the amount of the individual component gases extracted from the oil are indicative of the type and degree of the abnormality present. Investigations performed over the years have associated the presence of the following gases with the given fault conditions

[19]:

- **Hydrogen (H_2):** Large quantities are associated with partial discharge conditions.
- **Hydrogen, Methane (CH_4), and Ethene (or Ethylene) (C_2H_4):** Results from thermal decomposition of the oil.
- **Carbon monoxide (CO):** Produced by thermal aging of the paper.
- **Acetylene (C_2H_4):** Associated with an electric arc in the oil.

The above gases are the ones usually identified in gas chromatography and are generally referred to as the "key gases" for diagnostic purposes. The above results allow the following fault diagnosis to be made based on the presence of the indicated gases [19][20]:

- Overheated cellulose (>150°C) will lead to carbon monoxide, carbon dioxide and water being formed.
- Excessively heated cellulose (>1000°C) results in the formation of carbon oxides, water and carbonaceous materials such as tar. This leads to destruction.
- Overheated transformer oil leads to the liberation of hydrocarbon gases, most notably ethylene, ethane and methane.
- Under electrical stress conditions (partial discharges and arcing) oil decomposes into large quantities of hydrogen and lesser amounts of acetylene along with small volumes of light hydrocarbons.

The DGA results can be interpreted by using different methods, the guidelines of which are set out and listed in international standards [17][18]. In addition to making a diagnosis based on the concentration of key fault gases, fault diagnosis can also be performed based on the relative concentration ratios of the individual gases dissolved in the oil. Dornerburg [21] developed a method to judge different faults by rating pairs of concentrations of gases, e.g. CH_4/H_2, C_2H_2/C_2H_4, with approximately equal solubilities and diffusion coefficients. Rodgers [23] established more comprehensive ratio codes to interpret the thermal fault types with theoretical thermodynamic assessments. This allows faults to be assessed as being high, medium, or low temperature and ratio codes indicate if the fault is due to general overheating or an arcing discharge. The gas ratio methods are useful because they eliminate the effect of oil volume.

Another traditional tool used for assisting with the interpretation of oil analysis results is the Duval Triangle [24]. For the triangle method, gas concentrations are related to a position in a triangle whose area is divided into cause segments. In Duval's paper [24], examples are given of expected times to failure with certain levels of gases. A more recent paper by Allen et al. [49] shows that a general indicator of the age of a transformer is given by an

increasing rate of CO_2 production with time. This is then used to compare the relative "insulation age" with "nameplate" age for similarly loaded transformers.

In order to get a reliable interpretation, it is necessary to take into account not only the absolute values but also the production rates of the different gases as the rate of gas formation can be indicative of the severity of the fault. Moreover, the type of transformer under investigation should be considered when making the analysis. For example a generator step-up transformer shows a different pattern than a system transformer and an HVDC transformer with much solid insulation differs from a furnace transformer [14]. When an indication of a fault is found, detailed knowledge of transformer design and how it operates in the field is needed to make the correct localization and to give the most reliable recommendation.

The procedure of oil sampling, gas extraction, chromatographic analysis and data interpretation is typically performed annually by most owners of large power transformers. However the use of DGA on an annual time interval can inject unnecessary risk and a false sense of confidence about the continued, ongoing health of a critical power transformer as any rapid change in the transformers gassing characteristics will go unmonitored and undetected. Furthermore, a DGA test reflects only the present condition of the power transformer. It is unreasonable to expect the DGA test to provide any guarantee of status quo until the next DGA test takes place. As a result assumptions made about the ongoing good health of a critical and costly power transformer based on annual DGA testing can be misleading and at best very risky, particularly when confronted with rapidly evolving faults.

Other disadvantages of DGA include:

- The very large volumes of oil in which gases are generated causes dilution which can make detection difficult. For very low concentration variations, it is difficult to make a distinction between gases generated by a fault and those which may be caused by miscellaneous phenomena with no harmful effects [22].
- DGA is not useful for factory testing by a manufacturer as gases are generated in too small a quantity and their diffusion is limited on account of the short testing time [22].
- A gas chromatograph is complex to operate, requires a long time to analyse and requires a skilled operator leading to a high cost of analysis.
- Determining whether the fault gases come from degradation of the oil or the cellulose can be difficult with DGA. Because the latter is important as far as the long term health of the transformer is concerned, additional tests are needed to assess the degree of degradation of the cellulose or polymerisation of the paper [3]. Such tests are described

in 2.3.3 and 2.3.2.3.

- A prime disadvantage of DGA is that there is there are inherent delays between site sampling and subsequent diagnosis of the transformer state.
- DGA gives no precise information on the location of the insulation damage and it requires time to establish positive trends in the results obtained.
- DGA looks at gases dissolved in oil only. Other gas analysis methods are needed to look at other gases in the tank.

2.3.2.2 Total Combustible Gas (TCG) Analysis

Heat and partial discharge can lead to the generation of combustible gases. The concentration of these gases, especially hydrogen, dissolved in the oil gives a good indication of the extent of insulation degradation. Total combustible gas (TCG) analysis is used to detect the thermal decomposition of the oil and paper insulation into these gaseous components. The first portable TCG devices measured the presence of combustible gases in the transformer gas space by their heat of combustion using samples periodically removed from the gas space. Continuous TCG monitoring employs a thermal conductivity cell that measures the percent combustibles in a continuously circulating sample of the transformer gas space. The detection of 0.5% TCG initiates surveillance procedures [29]. When a portable TCG detector is used, a sampling interval of 4 to 6 months is customary.

2.3.2.3 Furanic Compound Analysis

When cellulose materials age as a result of thermal stress, liquid furanic compounds are generated as a degradation product. Furanic compounds are a family of chemical substances that differ in stability and production rates. The monitoring of furanic compounds by annual sampling of the oil and its analysis using high performance liquid chromatography (HPLC) has been used for condition monitoring on a routine basis for some years [4]. Generally furfuraldehydes (FFAs) are extracted from the oil either by solvent extraction or solid phase extraction and measured by HPLC using a UV detector [2].

It has been shown that there exists a relationship between degree of polymerisation (DP) and the concentration of furanic compounds [28], which allow for an indirect measurement of the degree of aging of the cellulose. The situation is however complicated by the fact that different types of paper show different production rates of furanes, and that the concentration is dependent on the mass ratio between oil and cellulose. As a result the relationship between the generation of these byproducts and the condition of the in-service paper has not been well established. Experimental tests have shown that the DP, or strength,

of paper insulation is inversely proportional to the FFA level, and the results from experiments indicate that a FFA level of 5ppm corresponds with a DP of 250 which is reckoned to be towards the lower limit for insulation strength. Although experience has shown that FFA in the oil can be reduced by on-site reprocessing and/or oil replacement, such oil changes will not alter the irreversible cellulose degradation which has given rise to the FFA [6]. In these circumstances, oil treatment will mask the underlying cause.

It has been suggested that furanic compound analysis can be as a method for determining the end-of-life of transformer insulation [14]. The work of Shroff and Stannett [27] reinforced by Carballeira [48] clearly shows the importance of measuring the FFA levels in insulating oils and how this can be a prime indicator of aging.

2.3.2.4 Expert Systems and Fuzzy Logic

Transformer fault diagnosis based on DGA results does not have a firm mathematical description and as a result are still in the heuristic stage. For this reason, knowledge-based programming is a suitable approach for implementing the diagnostic problem. Since the conditions under which fault gases dissolve in transformer oil are related to manufacturers, construction processes, loading history, volume of oil and oil in the sampling container, imprecision and incompleteness are characteristic of the fault diagnostic problem. As a result the effectiveness of existing DGA diagnostic methods is still unsatisfactory. As a step towards improving diagnostic methods, fuzzy information and knowledge-based expert systems using fuzzy set concepts [43][44] have been proposed.

Lin et al. [44] have developed a system that uses key gas concentrations and concentration ratios to make decisions based on forward chaining (event driven) and backward chaining (goal driven) inferencing. The system can diagnose incipient faults in suspected transformers and suggests appropriate maintenance actions. Fuzzy set concepts are used to handle uncertain concentration thresholds and ratio boundaries. The knowledge base was built using DGA data recorded over a ten year period and can be expanded by adding new data and experiences. More recently Huang et al. [45][46] have described a fuzzy DGA diagnosis system based on evolutionary fuzzy logic. Evolutionary programming is used to automatically modify the fuzzy if-then rules of the knowledge base and to adjust the corresponding membership functions.

Zhang et al. [47] have applied artificial neutral networks (ANNs) to the problem of transformer fault diagnosis based upon DGA results. Obvious and not so obvious (hidden) relationships are detected by the ANN and used to develop its basis for interpretation of DGA data. Through the training process, the ANN can reveal complex mechanisms that

may be unknown to a human expert. This is in contrast to expert and fuzzy-set systems that can only use explicit knowledge to establish a knowledge base and select membership functions.

2.3.3 Degree of Polymerisation (DP)

In the past the rate of degradation of paper insulation was measured by mechanical strength tests such as tensile, bursting and tearing etc. More recently a chemical measurement of the Degree of Polymerisation (DP) has been used [25]. Determination of the DP value of cellulose is a standard method for quantifying the degradation of cellulose. It is a measure of the average number of glucose rings in the cellulose molecules (see Figure 2.1). When cellulose ages thermally, the molecular chains are broken and when aging is far progressed, the paper becomes brittle and losses it's mechanical stability. The method is good for a quantitative measurement of thermal aging. The degree of polymerisation of paper varies from about 1300, for new paper, to approximately 150-300 for insulating paper at the end of its life [4].

DP is used to detect the following three mechanisms, each of which contributes to cellulose degradation in an operating transformer[1] [26]:

- **Hydrolysis (water):** The oxygen bridge between the glucose rings (see Figure 2.1) is affected by water, causing a rupture of the chain and leading to a reduction in the DP.
- **Oxidation:** Oxygen attacks the carbon atoms in the cellulose molecule to form aldehydes and acids, releasing water, carbon monoxide and carbon dioxide. As result the bonds between the rings are weakened, leading to a lower DP.
- **Pyrolysis (heat):** Heat contributes to the breakdown of the monomers in the cellulose chain, liberating gases, leading to a reduction in the DP.

The main drawback associated with DP tests is that a paper sample taken from the transformer is required. This is an intrusive action which requires qualified service personnel and the transformer to be taken out of service. Furthermore, the sample cannot be taken from inside the winding, but is instead normally taken from one of the high current leads in the upper part of the transformer [14]. An additional disadvantage of DP measurements is that they are labour intensive.

The thermal decomposition of both paper and oil may produce carbon monoxide, but paper is less stable, producing CO at lower temperatures than oil. Consequently, the ratio of CO_2/CO has been used in the past as an indication of paper decomposition. Further, as

[1] Modern oil preservation systems prevent entry of oxygen and water by sealing the tank while operating procedures are used to control the temperature.

cellulose ages, the chains of glucose rings in the molecules break up and release carbon dioxide, and water [9] in addition to carbon monoxide. The water attaches to the impurities in the oil and reduces oil quality, especially dielectric strength. The reduction in dielectric strength may lead to transformer failure.

2.3.4 Pressure Monitoring

Oil pressure can be used as an indicator of insulation deterioration. Pressure behaviour can be divided into the following three categories, depending upon the condition of the transformers insulation [30]:

- For a good transformer whose insulation has a low power factor: The pressure fluctuates with temperature, increasing in hot whether due to the expansion of the confined oil.
- For a transformer with moderate gassing and an insulation power factor that is increasing: The pressure increases with the power factor due to the self heating of the transformer
- For a transformer with excessive gassing: Once the oil becomes saturated with gases, they have nowhere to go except to form a blanket above the oil. As a result pressure increases proportionately, sometimes to several times the original value. Thus excessive pressure can indicate excessive gassing.

Although pressure can be used as an indicator of a bad transformer, ambient temperature effects need to be compensated out during the middle stages of failure. Temperature compensation is not needed during the final stages of failure, but because leaving a transformer in service until it has reached such an advanced state of deterioration is not advisable (due to premature failure), pressure monitoring often cannot be applied practically.

2.3.5 Dielectric Response

Dielectric response testing consists of analysing the relaxation of the insulation after the application of a low frequency sinusoid or DC. This method is used to determine the moisture content but has also been applied to determine aging. Measurements can be made in either the time domain (i.e. the recovery voltage [31]) or in the frequency domain, and it has been shown that the two methods reflect the same physical quantities [32]. Disadvantages of dielectric response testing include:

- The transformer must be disconnected from the power system.
- It is not possible to make a quantitative statement concerning the moisture content of the

transformer if no reference measurements for the transformer are available.

- The transformer design needs to be taken into consideration since the dielectric response also depends on the geometry of the active part and on volume ratios between solid and liquid insulation.

The dielectric loss angle procedure (tanδ measurement), is a special case of the dielectric response i.e. the response at 50 or 60Hz.

2.3.6 Low Voltage Impulse (LVI) Testing

Mechanical stresses produced by short circuit forces can distort and displace transformer windings. The distorting effects of short circuit forces may lead to catastrophic failure immediately, in which case diagnosis is trivial. However, if the windings merely displace, the transformer may to continue to function but in a much weakened state. The windings may subsequently fail due to insulation abrasion or during another short circuit on the connected system. Inadequate clamping arrangements may lead to winding movement under service conditions. Clamping may become inadequate due to insulation shrinkage and results in a weakened winding making the transformer vulnerable to failure due to winding abrasion or winding forces developed during service (e.g. at switch-on or upon external short circuit). The test techniques most widely used for assessing the degree of winding movement in power transformer are applied off-line. This section addresses the LVI test technique. Techniques based on leakage inductance and frequency response measurements are discussed in the sections to follow.

Winding deformation that is caused by lightning, switching faults, and system faults can be determined by low voltage impulse (LVI) testing. The technique involves exciting the resonant modes of the winding by applying a steep fronted impulse, typically 1.2/50μs. The time domain response at the remote end of the winding is then recorded and compared with prior recordings. Experience has shown that changes in the winding structure can be detected by comparing 'as new' responses with responses taken later. Interpretation of the changes in response is largely a matter of experience, aided by a knowledge of the winding arrangement of the transformer. Knowledge of the transformer winding being tested is desirable for the most effective use of the LVI method, and should be allowed for when selecting the measurements to be made [36].

When the LVI method was first proposed by Lech and Tyminski [37], one winding was impulsed and the induced current flowing to earth in the other winding was measured by means of a shunt. Subsequently it was found that greater sensitivity could be obtained with a circuit in which the difference is measured between the currents flowing to earth from two

phase windings that are simultaneously being impulsed (i.e. 2 primary windings). A differential circuit of this type is suitable for most measurements on three phase transformers, however it has limited application to single phase units, where instead the induced current approach is used. When measurements are made on a transformer using the LVI method, the service connections to the terminals must be disconnected so that the measurements are not affected by any changes in the layout or earthing of these connections.

Although LVI is recognised as being exceptionally sensitive, its application has been limited due to the difficulty in relating response alterations to the physical changes causing them. Because the waveshape and amplitude of the applied impulse affect the response, the application of LVI has also been limited by the practical difficulties of achieving noise free and repeatable results under site conditions [50].

2.3.7 Leakage Inductance

Leakage inductance measurements have traditionally been used to detect mechanical deformations and changes in winding geometry. As a result of a short circuit, the inner winding has a tendency to decrease in diameter whereas the outer increases. This leads to a higher leakage flux between the windings and thus a higher measured leakage reactance [14]. The relationship between winding displacement and changes in leakage inductance is recognised in [41], which sets a criteria at 2% change as being significant. However, the test, though useful can be insensitive to winding displacement [50].

A related technique has been developed by Hydro Quebec [51], that involves the measurement of stray load loss across a range of frequencies. The technique, referred to as frequency response of stray losses (FRSL) is based on the observation that axial winding displacement causes an increase in stray losses. For the FRSL test the transformer is short circuited on the secondary, while the primary winding is supplied with low voltage over a frequency range of 20-400Hz. The technique is considered [51] to be sensitive down to axial displacement of the order equivalent to winding separation although it is considered insensitive to radial displacement.

2.3.8 Frequency Response Analysis (FRA)

As discussed in 2.3.6, the low voltage impulse (LVI) method is used to detect winding mechanical deformations caused by short circuit fault currents and other mechanical stresses. An alternative method, frequency response analysis (FRA) [33], is based on the fact that should the spatial disposition of a winding alter then its distributed parameters will

alter and consequently so will its frequency response. The frequency response of a winding therefore directly reflects its spatial disposition.

The FRA method uses a sweep frequency generator to apply low voltage sinusoids at different frequencies to one terminal of a transformer winding. Typically the frequency sweep is performed up to a few MHz. Amplitude and phase signals from selected terminals of the transformer are recorded and used to determine voltage ratio and impedance transfer functions at each discrete frequency included in the sweep. Comparisons are then made between transfer functions determined before and after winding damage. The FRA is typically performed using a network analyser [33] and is used for large power transformers to provide fingerprint information at manufacture and when commissioned on-site. This data is then used as a future reference for comparisons with results obtained after winding deformation.

In applying FRA, the transformer must be physically disconnected from the buswork at all bushing terminals so as to prevent bus capacitance from effecting the FRA results [33]. As a result preparation time can be considerably longer than the test itself. Further, the resources required to carry out FRA testing may limit its application to one-off problem solving and as a preliminary measure to justify more expensive detanking.

Bak-Jensen et al. [34] have demonstrated that a transfer function determined by FRA provides a highly stable transformer model. As a result they have developed a model-based diagnostic procedure where a comparison is made between a reference transfer function and subsequent transfer functions. Sensitivity tests were developed to examine the relation between the transfer function and

- Insulating oil/grease: It is possible to detect a change in the quality of transformer oil/grease if this involves a change in the dielectric constant, ε_r.
- Core: It is possible to detect a change in the condition of the core if this involves a change in the total reluctance or total losses in the iron.
- Winding/coil insulation: It is possible to detect changes in the condition of the winding insulation if this involves changes in the winding capacitance or shorts between turns.

Disadvantages of FRA include:

- The instrumentation used can have a large effect on the transfer function. Results form Dick and Erven [33] show that replacing 50Ω coax in the measurement system with 75Ω coax can have an effect over a large range of frequencies. As a result standardised test equipment should be used.

- Thorough FRA testing on three phase transformers can involve many hours of testing. A Y-Y transformer for example has 8 terminals, so that many different transfer functions are possible.
- Because low voltage inputs are used for FRA, output signals as low as 20μV are obtained at some frequencies. Measurement of these low level signals, especially close to an energised bus in a substation, can be difficult. This can add unwanted uncertainty into the FRA technique.
- Strays in the measurement system can have an effect on the results at higher frequencies. These include parasitic capacitance effects and conductive loops within the measurement system that are prone to EMI pickup.
- Bushing capacitance can have a dominating effect on impedance transfer functions.
- Fault detection can only be achieved if a reference transfer function is available, although phase-to-phase comparisons may provide a reasonable fingerprint in the three phase case [35].
- The transformer under test must be removed from service.

Advantages of FRA include:

- Because the input signal is concentrated at a single frequency then effective narrow band filters can be used on the received signals to increase the SNR.
- It can also be used to determine the integrity of the winding insulation.
- Does not require the extensive calibration of LVI and is not subject to interference as is LVI.

2.3.9 Partial Discharge Detection

A partial discharge is an electric discharge that only partially bridges the insulation between conductors. These discharges occur in gas, usually air, when the voltage exceeds some limiting value and discharges the capacitance of the insulation with which they are in series. Solid insulation may be damaged where either or both ends of the discharge is rooted on an insulating surface. The early detection and location of partial discharges within power transformers is therefore important if degradation or incipient breakdown of insulation is to be avoided. Further, many experiences have shown that the insulation damage caused by internal partial discharge activity has become a main factor influencing the reliable operation of a power transformer. The detection and location of partial discharges in transformers during factory tests is well established and dealt with by current standards [41][40].

It is known that partial discharges produce a number of signals at different locations within a large transformer. These signals can be categorized as follows [42]:

- Discharge current in the transformer's neutral terminal.
- Displacement current through the capacitive tapping of a bushing.
- Ultrasonic/acoustic signals that emanate from the source of the partial discharge activity.
- Radiated RF signals.

Partial discharges occurring within the insulation inside a transformer initiate acoustic waves which travel in all directions and reach the tank walls. The use of acoustic and/or ultrasonic transducers installed on the tank walls to both detect and locate partial discharges has been used in both off-line and on-line applications. Localization of partial discharges is made acoustically using different triangulation techniques. This requires deep knowledge of wave propagation in different types of materials/liquids [38] and is a task for highly qualified experts. This technique is applied using the time interval between the appearance of a partial discharge (possibly detected using discharge current) and the sensing by a detector fitted on the tank wall. This allows the source-detector distance to be measured. Through the use of multiple sensors, several of these distances can be determined and triangulation applied to geometrically locate the source within the transformer. Because the transformer is not a homogenous medium, the speeds of propagation of the wave transmitted are dependent on the materials through which the wave propagates. This phenomenon must be taken into account when interpreting the results [22]. Acoustic detectors are used that continuously receive signals in the sonic and ultrasonic bands.

Another technique that has been used for locating the source of PD activity within a transformer is the profile comparison method. The profile comparison method is used to electrically locate a fault, independent of its geometrical position (e.g. the phase). The profile comparison method consists of injecting a known signal across two accessible points of a transformer and collecting the responses at selected points so that profile representing the transmission coefficients may be obtained. After a number of profiles have been determined, the transformer is energised and partial discharge levels are measured at the locations used to determine the profiles. By comparing new profiles with the former ones, it is possible to locate the source of the partial discharge [22].

On the practical side, noise suppression in a substation environment poses the largest challenge [22]. For in-situ measurements sometimes the electrical signal is too weak compared to the level of interference and therefore cannot be detected. However because the signals are repetitive, averaging can be used to improve the SNR. This allows the detection of very weak partial discharge signals that are buried in noise.

Knowledge of the spot where the fault is occurring offers the following advantages:

- When partial discharge location is determined during factory testing by a manufacturer, it is possible to open the transformer and repair the fault. This allows the manufacturer to assess the extent of the repairwork and perform the work after minimum dismantling.
- For the user, who may make a decision to continue operating the unit under regular supervision, based on this information, in order to wait for the most favourable time to carry out the repairwork. Or contrary, the user may use location information to decide to take the unit out of operation before exceeding the threshold , which may be destructive. In all cases, repairs can be made at a lower cost.

In the past, reliance has been placed on DGA for the initial detection of excessive partial discharge activity [7]. Only after excessive partial discharge activity was detected was the location of the partial discharge attempted. Techniques similar to those employed during factory tests have been used during on site off-line tests. Partial discharge measurement systems are discussed in Chapter 3.

2.4 Integrating Fault Diagnosis Methods

The methods presented in this chapter are used to identify transformer fault conditions before they deteriorate to a severe state. All of the methods presented require some experience in order to correctly interpret the observations. Researchers have applied artificial intelligence concepts in order to encode these diagnostic techniques. Many of these attempts have concentrated on only a single diagnostic technique and have failed to fully manage the inherent uncertainty in the various methods [35].

A better analysis would result by aggregating information from more than one of these techniques. All of these methods are imprecise and require experience in order to correctly interpret the observations. This inherent uncertainty in transformer fault diagnosis techniques has led several researchers to apply fuzzy set methods. In [44] and [52] fuzzy logic is used to implement DGA methods, while [53] describes an acoustic technique that applies fuzzy logic to represent uncertainty. Tomsovic et al. [35] describe an approach that integrates different diagnostic techniques and systematically manages uncertainties that arise from the different diagnostic techniques. In the developed expert system, each diagnostic method is represented by a rule base. Within each rule base, conflicts arising between rules are resolved to find the most consistent solution. Finally the diagnoses are combined into a single analysis where more weight is attached to more certain diagnoses. The system is robust to missing or inaccurate data and can easily be expanded to

accommodate new diagnostic techniques.

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Chapter 3

TRANSFORMER INSULATION CONDITION MONITORING

This chapter reviews trends and recent developments in on-line condition monitoring of power, distribution and instrument transformers. Monitoring systems based on temperature measurements, differential relays, transformer modeling, partial discharge detection, dissolved gas analysis, and other methods are discussed and some currently available monitoring equipment is described. Discussions on the presented techniques include existing systems and practices along with their capabilities and success rates.

It is desirable to monitor the condition of insulation in power transformers as this allows improved preventative maintenance to be applied which leads to an increase in the life of the transformer. Because the assessment of the remaining life of a transformer is one of the most important issues related to monitoring, a section on transformer life assessment is presented. Sections on transformer impulse testing and the transfer function method have been included as this material directly relates to the transformer insulation condition monitoring system developed by the author.

3.1 Overview

There are two main reasons for installing monitoring equipment on transformers. First, by monitoring the important functions of a transformer, developing faults can be detected before they lead to a catastrophic failure. Second, it can allow for a change from a periodic to a condition based maintenance program, leading to reduced maintenance costs. Furthermore, because the main part of the transformer population is old[1], many transformers may reach the end of their lifetime in the next few years, possibly leading to cascade failures.

[1] In many European countries, essential power system components were renewed after the second world war and as a consequence there are a lot of power transformers that are over 30 years of age [62].

Monitoring equipment, which per definition is on-line and permanently mounted on the transformer, must primarily be reliable. In general, lower cost systems supply a reliable warning signal without on-line analysis and diagnosis. Diagnosis methods presented in Chapter 2 usually follow up an alarm condition. Monitoring equipment should be designed for field installation on transformers already in operation.

The benefits of condition monitoring can be summarised as follows [41]:

- Reduced maintenance costs
- The results provide a quality control feature
- Limits the probability of destructive failure and thus leads to improvements in operator safety and quality of supply
- Limits the severity of any damage incurred thus preventing consequential repair activities
- Can identify the root cause of failure
- Information is provided on the transformer operating life, enabling business decisions to be made either on transformer refurbishment or on asset replacement.

3.2 Transformer Life Assessment

The assessment of the remaining life of a transformer is one of the most important issues related to monitoring and diagnostics. The ultimate question to be asked is how many years a unit has before it fails i.e. when has its end-of-life (EOL) been reached where EOL is taken to mean that the transformer is no longer able to fulfill its required function economically.

Distinctions can be made between technical, strategical and economical EOL [45]. It is seldom that transformers are replaced for technical reasons only. The main reasons for taking transformers out of service are cost related as the total operating cost is minimised. Strategic reasons arise from changes in load patterns and changes in voltage level etc. Second, it is important to distinguish between the technical EOL of the insulation materials and the EOL of the transformer itself. Recent studies have revealed that no correlation exists between transformer EOL and load [45]. This is most likely due to the use of pedantic maintenance procedures rather than suggesting that thermal aging of the insulation has little affect on the transformer EOL

The technical EOL of a transformer is a function of many factors including design,

historical events, previous operating conditions, its present state and future service conditions. Most methods proposed for estimating EOL focus on only one of these aspects, the present state of the insulating material. Furthermore, load and temperature are not the only factors that should be taken into consideration. The number of experienced short circuits and overvoltages, design weaknesses, repairs and transportations between sites will influence a transformers ability to perform its function and therefore should be taken into account. It is therefore important that utilities keep historical records concerning the operating conditions if accurate EOL predictions are to be made.

A subject of major concern to the utility industry is projected equipment life. For transformers, utilities apply industry loading guides [7] to assist in establishing load practices that will not unduly jeopardize life. Loading guides provide equations to enable estimation of insulation hottest spot temperature as a function of load, leading to a temperature/time relationship that can be used to compute consumption of life [52]. It must be noted that transformer loading guides define the life of the material in the insulation system as it is influenced by temperature, not the functional life of the transformer, which may be affected by mechanical and dielectric stresses.

If an end point for insulation life is to be defined, it must be done in terms of a measurable physical characteristic of the material. In the past 50% deterioration of the tensile strength of the paper has been used as end-of-life indicator [52]. An alternative end-of-life definition has been suggested by some investigators, namely the degree of polymerisation (DP) discussed in 2.3.3. This approach seems to have merit as reduction in the DP corresponds with a deterioration of mechanical properties as discussed in 2.3.3. Bozzini [49] suggests that a DP value of 100-150 be used to indicate the end-of-life of the insulation.

The work of Allan [4][5], on the distinction between nameplate age and insulation age is significant in assessing the remaining life of transformers. His papers and also that of Darveniza et al. [6] show how micro-samples of paper insulation from transformers in service can be used to yield information on the aging of the insulation.

3.2.1 Thermal Measurements

It is essential to know the maximum temperature reached by the winding insulation if a transformer is to be loaded efficiently and it's insulation life expectancy calculated. In the past thermocouples and RTDs have been used for winding temperature measurements [54]. However a major difficulty encountered in the practice is that the temperature is generally not uniform throughout the winding due to localised variations in the effectiveness of the coolant. Further the locations of the highest temperature, the hot spots, are often within the

winding and inaccessible to external probes. Techniques for estimating the points of highest temperatures in windings based on temperature measurements at other locations have therefore been developed. The thermal image temperature indicator, which produces a hot spot estimate based on oil temperature and load current is one of the most widely used instruments [1][56]. Other instruments and techniques use factors such as average winding temperature, bottom oil temperature, and top oil temperature and from them estimate hot spot temperature [56]. However these methods are inaccurate and because allowing hot spots to exceed certain temperatures dramatically increases the risk of breakdown, conservative loading policies have been applied. Accurate knowledge of the true hot spot temperature leads to more improved transformer utilisation and better life expectancy estimates. The relationship between insulation life expectancy and operating temperature is discussed in 2.1.1.

The above limitations can be overcome by measuring the winding temperature directly. However a measuring unit must be produced which is rugged and small enough to be embedded in the winding without causing too much disturbance. Most importantly such a device must in no way weaken the electrical insulation of the transformer. Recently, implanted temperature measurement devices fitting these criteria have been developed and used to directly measure winding insulation hot spot temperatures. The main techniques used include:

- A vapotherm capsule: This method uses the vapour pressure of acetone contained in a capsule embedded in the winding. Temperature is measured by transmitting the vapour pressure to pressure transducer via a capillary tube filled with oil [53].
- Fibre optics: Devices based on temperature dependent light phenomena using optical fibres for light transmission appear promising. Hampton et al. [53] have developed a system where laser light is polarised and transmitted to a quartz block in the winding. Its plane of polarization is rotated by the quartz, the angle being dependent on the quartz temperature. The emerging light is analysed and the temperature determined. Another system put forward by Lampe et al. [54] transmits light to a semiconductor sensor, which absorbs the light and retransmits it at another wavelength where the change in wavelength is determined by the sensor temperature.

Fibre optic hot spot detectors are being used in new and repaired transformers. A CIGRE survey [57] reported that two to eight sensors would be adequate if placed in the winding where the higher temperature is expected.

It is well known that voltages and currents with frequencies above 50Hz result in additional heating in iron-cored devices like transformers [58]. Because the increasing use of harmonic

loads on power systems has resulted in transformers running at rated or higher temperatures at less than full load current [55], monitoring hot spot temperatures can be valuable if loss of life is to be avoided [59].

3.3 Developments in On-Line Systems

To detect abnormalities in transformer insulation systems, various condition monitoring techniques such as partial discharge detection, dielectric loss angle measurement and gas-in-oil analysis are used, as discussed previously. The problem with these conventional off-line monitoring techniques is that they are periodic, labour intensive and require the transformer to be taken out of service for some time. Furthermore, in the past it has not always been possible to perform these tests at sufficiently regular intervals due to resource and operational constraints. As a result, emphasis has recently been placed on the development of on-line systems to reduce the number of transformer failures that have been experienced throughout systems around the world. In the past many such systems have not been possible or practical with the use of conventional analog instruments, but the advent of digital data acquisition and processing equipment has enabled the development of on-line diagnostic and measuring systems suitable for use in a power system.

The advantage of on-line systems is that they give immediate indication that something is wrong, perhaps in time to remove a transformer from service and prevent a catastrophic failure. However as the cost of removing and replacing a large power transformer increases with its capacity and the remoteness, the decision to remove a power transformer from service can imply an expense of several tens of thousands of dollars and is justified only by a high degree of confidence in the predicted imminent insulation failure given by such systems.

Assessment of the condition of the HV insulation of transformers in service has long been of major concern to public utilities, and many attempts have been made to predict incipient insulation faults and extend transformer life. This section gives an overview of recent advances made in the development of on-line condition monitoring equipment used to detect faults, monitor insulation condition and to evaluate the age of insulation in power, distribution and instrument transformers. The systems presented fall between the following two extremes:

- Expensive, complex systems that can automatically monitor several parameters, process the acquired data, determine rates of change of parameters, establish correlations between parameters and transmit the results to a control center.

- Simple automatic systems that record a single parameter, signaling exceeded levels to the substation operator.

Systems of the later type have found various applications e.g. for monitoring hydrogen in transformer oil [32] or detecting partial discharges [33]. However the results of single parameter monitoring, although useful to the person in charge of the substation apparatus, have an inherent limitation in that they cannot answer the basic question: ***should the transformer be removed from service now to avoid insulation breakdown?***

3.3.1 Transformer Insulation Life Monitor

A prototype system has been developed by ESKOM to measure the life usage, and conversely the remaining life, of a transformer [1]. The design philosophy of this instrument is based on the insulation life equations, used to prepare the "Loading Guide for Oil-Immersed Transformers" as given in IEC-354 [7]. To summarise, the insulation life is primarily a function of the insulation temperature and time as defined by Arrhenius's Law [3]

$$L = Ae^{B/T} \qquad (3.1)$$

where L is the life, T is the temperature, and A, B are constants. When applying Eq. (3.1), the maximum insulation temperature (hot spot temperature) must be used. Because the precise location of the hot spot is never known, then the hot spot temperature cannot be measured directly. As a consequence of this the instrument developed by ESKOM uses an estimate based on the oil temperature at the top of the tank and the loading (i.e. load current) of the transformer. Because of the logarithmic nature of Arrhenius's Law, the estimated transformer life is very sensitive to the inaccuracies in the measured parameters (temperature and load current). Dewe et al. [1] found that hot spot temperature estimate must be within 1.5% to ensure a life estimate accuracy of 20%.

The developed prototype system monitors a transformer in service and outputs the number of life hours used onto an LCD display. The peak and average temperature and load current can also be displayed.

3.3.2 Buchholz Relay

Power transformers are often protected by gas accumulation devices commonly called Buchholz relays. Gas generated in the transformer oil rises to the highest point in the oil where it is trapped in the accumulation chamber of the device. When a predetermined amount of gas has been accumulated, this information is transmitted via electrical signals to

the devices protection relay. A Buchholz relay is also capable of detecting oil leaks in a power transformer.

When a transformer gives off a Buchholz relay gas warning, information may be obtained on the origin of the fault producing the gas emissions, depending on whether the Buchholz gases are balanced or not with the gases dissolved in the tank oil [44]. In performing this technique, an oil sample is often taken from the bottom of the tank.

3.3.3 Differential Relay Protection

Relays that use over current, over flux and over heating principles protect transformers against overloads and externally applied conditions. Differential relays are used to protect transformers against internal faults [10]. These relays convert the primary and secondary currents to a common base and compare them. During normal operating conditions, the differences between the currents are small and are due to magnetising and core loss currents. The differences are also small during external faults although they are larger than the differences during normal operating conditions. When either an internal fault or magnetising inrush (a transient that occurs during energisation) occur, the differences are large. Conventional relays use the 2^{nd} and/or 4^{th} harmonic components of the difference currents, which are larger for magnetising inrush, to distinguish between the two conditions. This prevents the relays from operating during magnetising inrush. During the last fifteen years progress has been made in the design of microprocessor-based differential relays. However these relays have been known to operate during some magnetising inrush conditions and are not very sensitive to turn-to-turn faults.

Sidhu et al. [8] describe a microprocessor based differential relay that can detect winding faults in single and three phase transformers. Their system accomplishes this by employing an algorithm that compares measured primary voltage(s) with primary voltage(s) calculated in terms of the transformer's secondary voltage(s), primary current(s) and secondary current(s). During normal operation and under external fault conditions there is little difference between the measured and calculated primary voltage(s). Both internal faults and magnetising inrush cause a large differences. However for magnetising inrush the difference only lasts for a short time and they use this to prevent the tripping of the transformer. The system was used in a laboratory setup to detect phase-to-phase faults and phase-to-ground faults for a three phase transformer. For these types of faults the system tripped the transformer in less than 20ms. More recently, artificial intelligence methods such as fuzzy logic [11] and neural networks [12] have been applied to differential relay protection systems to prevent them from tripping the transformer during magnetising inrush.

Degens and Langedijk [17] describe an on-line microprocessor based differential protection system that operates similarly to a conventional system. In a conventional system transformer overload can cause false tripping due to the increase in magnetising current. Degens and Langedijk prevent this by detecting the presence of 5^{th} harmonic components.

An advantage of using a microprocessor based system is that additional protection schemes can easily be incorporated. Degens and Langedijk [17] take advantage of this by including additional software algorithms that perform the following protection functions:

- Earth fault protection at primary and secondary sides: Based on Kirchhoff's current law.
- Primary to secondary winding fault protection: Based on Kirchhoff's current law.
- Inverse time current protection: Used to protect against overloads and overcurrents and is based on numerical integration.

A disadvantage with differential relay protection is that preventative techniques to avoid outages based on early detection of faults cannot be applied.

3.3.4 Model-Based Monitoring

MIT has developed an adaptive, intelligent monitoring system for large power transformers [9]. The system consists of a collection of data acquisition modules that monitor temperature, gas content and partial discharge activity. A connection to the system can be made through a modem which allows MIT personnel to operate the system and examine the data independently of the host utility. Each module uses model-based monitoring which compares measured data with that predicted from a model and generates a residual signal (the difference between the measurement and the prediction). When a residual signal exceeds a predefined range or changes faster than a given rate, messages are generated to appropriate personnel via a paging system, to indicate that a problem has developed.

An adaptive transformer model based on parameter estimation is used. This facilitates transformer condition monitoring on multiple time scales and allows for differences between individual transformers. When testing the system in the field, the following problems were experienced:

- The IEEE temperature model used does not properly account for variations in ambient temperature[1].
- When a transformer cooling pump was activated the gas module predicted a drop in gas content (a model based on temperature is used). The resulting increase in the residual

[1] A modification based on the correlation between the error in the existing model and ambient temperature has been proposed [60]. Improved results suggest that the proposed model is better suited to model-based on-line monitoring systems.

caused the system to generate a message when no fault had developed.

3.3.5 On-Line Partial Discharge Detection

Many experiences have shown that the insulation damage caused by internal partial discharge activity has become a main factor influencing the reliable operation of a power transformer. Further, partial discharge erosion of the insulation of high voltage plant is one of the main deteriorative mechanisms leading to early failure. As it is suspected that partial discharges of high magnitude develop shortly before a major failure, continuous monitoring of large and/or critically located transformers is very desirable. This section presents a number of on-line systems that have been designed to detect partial discharge activity in power transformers and other HV apparatus.

It is known that partial discharges produce a number of signals at different locations within a large transformer. These signals can be categorized as follows [16]:

- Discharge current in the transformer's neutral terminal.
- Displacement current through the capacitive tapping of a bushing.
- Ultrasonic/acoustic signals that emanate from the source of the partial discharge activity.
- Radiated RF signals.

Recently on-line systems that detect partial discharge activity have been developed and applied in the field. Because these systems are required to operate under severe noise and interference conditions within a substation environment, transducers are often used that detect two or more of the above signals. As a result, systems are able to apply noise-rejection algorithms to differentiate partial discharge activity from noise and interference when signals are only present at the output a one transducer type. A brief summary of some of the recent progress in the development of on-line partial discharge detection systems is now presented.

Multichannel pulse height analysers have been used for PD analysis since the 1970s, mainly for the measurement and sorting of discrete pulse heights and corresponding discharge rates. The current trend in digital recording is the substitution of much of the pulse height analyser hardware with personal computer oriented software. Many hardware and software systems have been described in the literature [15][16][19][20][21][22][23][24][25][26]. Basically, all of these systems use some method to record pulse heights along with the corresponding applied voltage magnitude and phase. The sophistication of the hardware determines the accuracy and resolution of the measurement of these parameters. Software enables other parameters to be determined and the results to be displayed in various ways.

Some selected on-line partial discharge monitoring systems are now examined.

Allan et al. describe an on-line partial discharge testing device used for testing substation instrument transformers [13][14]. The system is used principally as a screening tool to detect abnormalities that are confirmed by more definitive and expensive techniques such as gas-in-oil analysis. The system was later modified to incorporate dielectric loss angle measurement when monitoring substation CTs and bushings, as this provides a measure of HV insulation deterioration over a period of time. The instrument determines the dielectric loss angle of the insulation by finding the phase difference between two 50Hz sinusoids measured at each end of the insulation. A zero crossing detector converts each sinusoid to a digital signal so that logic circuitry and a microprocessor can be used to find the phase difference. The system detected deterioration in 110kV and 132kV CTs and conventional off-line tests performed with these units confirmed that the insulation was in an advanced state of degradation.

Zhu et al. and have developed an on-line computer aided system for the detection of partial discharges [15]. Acoustic and current transducers are used to detect partial discharge activity. The acoustic transducer consists of a piezoelectric sensor, a preamplifier and a filter. The filter is able to remove interfering signals from magnetic and mechanical sources, based on knowledge of the frequency spectra of the acoustic emission signals. The current transducer consists of a clip on CT, a preamplifier and a filter. A clip on CT was used to sense partial discharge current pulses as a current measurement shunt connected in series could not be used under service conditions. The bandpass response of the CT and the filter were used to remove unwanted interfering signals. A single fibre optic channel along with frequency division multiplexing was used to transmit signals from three acoustic transducers and a current transducer to a PC, located in a control room some hundreds of meters away. An acoustic wave propagation velocity in oil of 1.4mm/μs along with the time delays between the current and acoustic signals is used by the PC software to locate the partial discharge source. The locations of partial discharge sources found during transformer repair agreed with those predicted by the system.

Unsworth et al. [16] have designed an on-line partial discharge monitor that consists of ultrasonic and RF transducers, signal conditioning electronics, digital signal processing and a display monitor. As the transducers are mounted inside the tank of the transformer they have been designed to operate as follows:

- In the corrosive medium of mineral oil
- At temperatures up to 120°C
- In the presence of strong 50Hz electric and magnetic fields

- Reliably for a long period of time as removal is difficult

Similarly to the system described by Zhu et al., location information is determined by using the RF signal as a time reference and measuring the delay to the ultrasonic signals.

Insulation deterioration due to partial discharge activity is not only a problem in power transformers. VanHaeren et al. [18] discuss insulation failures in metalclad switchgear and develop a prototype on-line system that detects partial discharge activity by monitoring for ultrasonic and RF signals.

A computer based on-line partial discharge detection system is described by Kurtz et al. [38]. The system uses split core high frequency CTs (insensitive to power frequency currents to avoid saturation) on the neutral leads of a bank of substation CTs to detect partial discharge activity. Detected current pulses are digitised and fed to a CPU for processing. The system is able to achieve noise-rejection by determining the direction of the detected current pulses. If current pulses are detected in the same direction in the neutral lead of each CT, they are rejected as noise. Partial discharge activity is identified in a CT when the detected current pulse travels in a direction opposite to that of the current pulses in the other CTs in the bank.

3.3.6 Hydrogen Monitoring

A on-line hydrogen monitor has been developed that measures hydrogen content in oil in ppm [36]. The device works best when it is mounted close to the windings in such a way as to maximise oil circulation to it. If this ideal mounting cannot be attained the device will not be very accurate, but will still give an indication within a few days of a large increase in hydrogen i.e. more than a few hundred ppm. The device is easily interfaced to microprocessor or computer-based protection systems although it has been reported that the hydrogen reading fluctuates somewhat with temperature excursions [34].

On-line hydrogen gas detectors are in general based on one of the following extraction systems [50]:

- **Vacuum suction system:** Gas is extracted by reducing the pressure of the space above the oil surface. A typical realisation uses a piston arrangement. Inoue et al [50] have shown that the extraction efficiency of a vacuum based system is greatly affected by the amount of residual air in the oil, increasing with increasing amounts of residual air. Because the amount of residual air contained in transformer oil may greatly vary from one transformer to another, a high vacuum and long extraction times are an essential requirement.

- **Permeable membrane system:** These systems employ polymeric membranes which in general have the property of letting only gases pass through them, stopping liquids. Some large transformer monitoring systems in service already use gas permeable membrane systems to extract dissolved gases for the detection of internal problems [51]. A problem with the gas permeable membrane system is that it takes several tens of hours for the hydrogen gas concentration in the gas chamber to reach equilibrium [50]. As a result its slow extraction time makes it unsuitable for use in a portable instrument designed to take quick field measurements.
- **Air blow system:** Air blow systems take advantage of the fact that the extraction efficiency increases with increasing amounts of residual air in the oil. Two air blow methods have been used [50]. In one method, air is blown into the oil and the air passed through the oil is collected. This requires a large amount of air to be collected to achieve good extraction efficiency and therefore does not allow a compact system to be designed. In the second method, a given amount of air is repeatedly circulated through the oil until an equilibrium is reached between the hydrogen gas concentration in the oil and in the air space of the device. Systems based on this method can be realised in a compact size. Advantages of the air blow system include an extraction time of a few minutes at most and an extraction efficiency independent of oil temperature (i.e. transformer loading).

Inoue et al. [50] have developed an air blow system that uses a SnO_2 sensor to measure hydrogen gas concentration. The measurement technique is based on the fact that hydrogen gas absorption changes the electrical resistance of the sensor. The sensor output is almost unaffected by the presence of other gases and is in close agreement with results obtained by gas chromatography.

3.3.7 Monitoring Other Gases in Oil

For a number of years, on-line sensors for detecting hydrogen (mainly indicative of partial discharges, but also arcing) have been available on the market e.g. the Hydran sensor from Cyprotec. These sensors are most sensitive to hydrogen, but also measure other combustible gases to a certain extent. The readings are to be regarded as warning signals, and a conventional gas-in-oil analysis should be performed after an alarm. Further, the risk of missing a beginning fault due to long sampling intervals is reduced considerably.

Recently, efforts have been made to develop on-line sensors that measure individual concentrations of several gases. Such sensors are also to be regarded as warning systems that give a better indication of the type of the fault, and will also give warning for heating of cellulose that present sensors do not. Examples are the developments made by ABB (metal

oxide technology) and by Micromonitors (metal insulator semiconductor technology). As of June 1996, both techniques were in the field prototype stage waiting to be commercialized.

The Hydran sensor uses a selectively permeable membrane and a miniature electrochemical gas detector. Hydrogen dissolved in the oil permeates through the membrane and reacts with oxygen from the ambient air. This reaction generates an electrical current that is measured as a voltage drop across a load resistor. A thermistor is embedded in the sensor for temperature compensation. Recent developments made to the sensor have enabled the detection of carbon monoxide, making it possible to monitor degradation of the solid insulation [48]. The advantage of the Hydran sensor is that it has no moving parts and the gases under analysis are the fuel required to energize the sensor, thus eliminating the need to replenish an internal agent.

Hydrogen and carbon monoxide are the first fault gases to form as an evolving fault initiates and increasing levels are true early signs of transformer dielectric breakdown and incipient failure. Together they represent the early warning indicators for both oil and cellulose type dielectric failure modes. On-line sensors, such as the Hydran sensor from Cyprotec, have been developed to continuously monitor for increased levels of these gases. DGA testing is performed when alarm signals are activated by these sensors.

To improve the detection capabilities of oil analysis techniques, the use of on-line Dissolved Gas Analysis (DGA) equipment has been looked at. However the cost of such equipment can be prohibitive and therefore may only justified on very high MVA rating transformers or as a semi-permanent installation on a problem transformer. Portable field DGA test sets can be used but do not have the precision of laboratory based equipment. These field sets can detect the presence of the primary gases (namely H_2 and CH_4) and identify the need for more detailed analysis.

3.3.8 Temperature

The hot spot of the winding is the limiting factor for the load capability of the transformer. Conventional temperature measurements are not direct, instead the hot spot is indirectly calculated from measurements of oil temperatures and load current. As an alternative, fiber optic temperature sensors can be installed in the winding when the transformer is manufactured. Two main types of sensors have been used, fibers which measure the temperature at one point [46], and distributed fibers which measure the temperature along the length of the fiber [47]. None of these are low cost systems, in particular, the distributed fiber sensor is costly to install and can be applied only for new transformers. Further information on temperature monitoring devices is presented in 3.2.1.

3.3.9 Other Systems

Other types of on-line sensors have also been investigated. Examples of such systems are on-line measurements of the moisture content of the oil, static charge in oil and pump monitoring. On-line measurements of the moisture in the cellulose by optical fiber techniques are also being studied. In general, these systems do not have a strong coupling to important and frequent failure modes.

A continuous transformer oil processing system was developed by Lampe and Spicar [27] to restore the dielectric strength of HV insulation showing signs of deterioration. This processing unit effectively removes oxygen dissolved in the oil and also metallic and dielectric impurities, thus preventing the evolution of an internal fault.

A microprocessor-based on-line transformer monitoring system has been developed by Poyser et al. [28][29]. The system uses sensors that measure top oil temperature, winding current, relative corona (based on acoustic waveguide developed by Westinghouse [30]) and gas in oil. Inputs to the system that indicate oil level, oil flow in cooling system and status of the cooling system are also processed. The system has been designed so that it can be extended when new or improved sensors, transducers and signal conditioning equipment become available. However as the system is fairly complex, reliability and cost may limit prospective applications.

Malewski et al. [31] describe the design of an automatic diagnostic system for large power transformers in service. Sensors were developed to measure overvoltages, partial discharge activity and gas in oil. The principle of operation of the system consists in correlating overvoltages and overcurrents with deterioration within the transformers insulation, as detected by the partial discharge and gas in oil sensors. The system also allows the operator to compare the high frequency spectral characteristics of fast transients with the frequency characteristic of a transformer winding so that dangerous internal winding resonances can be detected.

The power factor of electrical insulation is recognized as a good indicator of its quality and future serviceability. Cummings et al. [34] have developed an on-line microprocessor-based system that detects insulation deterioration within a substation CT by continuously monitoring the insulation power factor and capacitance. The system also measures temperature and applies a correction to estimate the internal temperature of the insulation. The estimated temperature is then used in power factor calculations to make temperature corrections [35]. The authors claim that temperature corrected power factor gives the best indication of long term changes in the CT, but that uncorrected power factor is the best

forecaster of imminent failure. Data supplied to the microprocessor from a commercially available hydrogen monitor and an oil pressure transducer was also used to detect insulation deterioration.

Other methods which have been tried and show some promise for detecting destructive trends or imminent failure include pressure monitoring and an extremely sensitive relay which looks at insulation current.

3.4 Transformer Impulse Testing

Voltage surges have always occurred on transmission systems and these surges, whether arising from lightning or switching, are liable to be propagated along transmission lines and into the windings of a transformer. To prevent breakdown of the transformer and interruption of the supply, transformer insulation systems must be designed to withstand surges with peak values that are many times the normal working voltage of the system.

For many years voltage impulse testing has played an important role in the development of the modern power transformer. Voltage impulses produced in a laboratory to simulate lightning and switching surges are used to obtain the surge withstand characteristics of power transformer insulation systems. The following standardised tests are now common practice on new power transformers:

- **Standard impulse test:** This includes the application of one calibration impulse at between 50% and 75% of the Basic Insulation Level (BIL), followed by three impulses at the BIL. Here the BIL refers to the peak voltage of the test impulse, which is related to the highest expected system overvoltage.
- **Chopped impulse test:** This test is applied according to the following test sequence:
    1. Application of one full wave at between 50% and 75% of the BIL
    2. One full wave at the BIL
    3. One or more chopped waves at between 50% and 75% of the BIL
    4. Two chopped waves at the BIL
    5. Two full waves at the BIL

Both tests employ a 1.2/50μs wave shape where 1.2μs is the 10% to 90% rise time and 50μs the time that it takes for the impulse to decay to 50% of its peak value. The chopped impulse is obtained from the 1.2/50μs wave shape by chopping the voltage after 2 to 6μs, thereby simulating an incoming surge chopped by a flashover of the coordination gaps close

to the transformer.

Voltage oscillograms are recorded for all tests along with one or more of the following:

- The current flowing in the earthed end of the winding under test, viz. the neutral current.
- The total current flowing to earth through a shunt connected between the tank insulated from earth and the earthing system, viz. the tank current.
- The transformed voltage appearing across another winding.

Detection of a breakdown in the major insulation of a transformer is usually made by comparing the voltage oscillogram recorded at the BIL with that obtained during the calibration test at the reduced level. Additional indicators used to detect faults are:

- Any change in the wave shape observed by comparing the full wave voltage oscillograms taken before and after a chopped impulse test.
- Any difference between the full wave voltage oscillograms and the chopped wave voltage oscillograms up to the time of chopping.

A breakdown between turns or between sections of a coil is, however, not always readily detected by the examination of voltage oscillograms and it is to facilitate the detection of this type of fault that the current or other oscillograms are recorded, as listed above. A comparison is then made between the neutral current oscillograms recorded at the BIL and at the reduced level for the standard impulse test. This is however based on the assumption that the winding impedance does not vary at voltages equal to the BIL and below. Assuming a constant shape for the test impulse over the test voltage range, the neutral current is then expected to have the same shape, provided that the transformer behaves linearly. Any nonlinearity observed at the higher test voltages implies an internal fault in the winding, which can be revealed by a usually minor difference between the compared current oscillograms.

Current oscillograms may give an indication of the position of a fault by a burst of high frequency oscillations or a divergence from the no fault wave shape. Since the speed of propagation of the wave through a winding is about 150m/μs, the time interval between the entry of the wave into the winding and the fault indication can be used to obtain the approximate position of the fault, provided the breakdown has occurred before a reflection from the end of the winding has taken place. Distortion of the voltage oscillograms may also help in the location of a fault but it generally requires a large fault current to distort the voltage wave and breakdown is then usually obvious.

The following difficulties and shortcomings are encountered with the testing procedures

detailed above:

- Any differences in the shape of the applied voltage impulse due to the impulse generator producing a slightly different impulse at the full and reduced levels, will cause a difference between the neutral current oscillograms, which according to the above testing procedure, may be incorrectly interpreted as a winding fault.
- Due to the difficulty in accurately controlling the chopping time, recorded neutral current oscillograms cannot be compared for the chopped impulse test.
- The subjective way of interpreting the differences between observed oscillograms can lead to controversy as there is no generally recognized evaluation criteria.

As impulse tests are usually carried in the final stage of the manufacturing chain, the failure of a transformer due to insulation failure has serious financial implications. It is therefore important to avoid the above problems and develop a reliable test procedure. The transfer function method eliminates the above problems and is therefore an improvement over the conventional testing procedures discussed here.

3.5 Transfer Function Method

Figure 3.1 shows a simplified circuit representation of a power transformer winding where M_i represents the mutual inductance between two winding elements separated by i-1 elements. Such a model has limited application in trying to model the high frequency behavior of the winding due to the decrease in the permeability of the iron core with increasing frequency, but is useful for illustrating the transfer function concept.

According to linear circuit theory the input and output of the 2-port network in Figure 3.1 are related according to the convolution integral

$$i(t) = \int_{-\infty}^{\infty} v(\tau)h(t-\tau)d\tau \qquad (3.2)$$

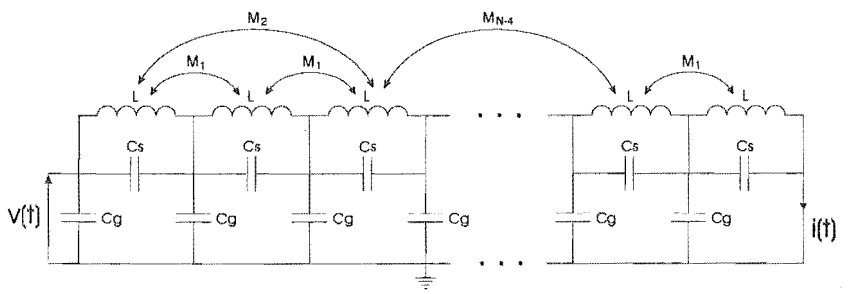

Figure 3.1 Simplified winding equivalent circuit

where h(t) is the winding impulse response. The transadmittance function H(f) can be determined by transforming Eq. (3.2) into the frequency domain and rearranging to produce

$$H(f) = \frac{I(f)}{V(f)} \qquad (3.3)$$

The transadmittance function thus characterizes the winding and any changes that take place in the winding insulation condition due to deterioration are reflected as transadmittance function changes. In general the transadmittance function is a complex quantity and its magnitude can be determined by dividing the magnitude of I(f) by that of V(f) while the phase is determined by subtracting the phase of V(f) from that of I(f).

It is important to state at this point that the transadmittance function is often referred to rather loosely in the literature as a transfer function. Because of this the technique introduced in this section has become known as the transfer function method. For consistency with the literature the transadmittance function defined above will be referred to as a transfer function throughout the rest of this chapter.

A typical test setup employed to determine the transfer function records both v(t) and i(t) illustrated Figure 3.1. The transfer function is then readily determined by applying Eq. (3.3). The transfer function method consists of comparing winding transfer functions obtained at the full and reduced test levels. The transfer function method relies on the assumption that the transformer impedance is linear for test voltage levels equal to and below the BIL, as is the case for impulse testing. The transfer function method and the impulse testing methods of the previous section only differ in the processing of the recorded data.

The transfer function can be determined through the use of the impulse testing techniques discussed in 3.4 [40] or by using the frequency response analysis techniques of 2.3.8 [42]. It is shown in [43] that the transfer function may be regarded as a "signature" of the transformer and is independent of the waveform applied. Transfer function analysis offers the additional advantage of fault identification and location. Bak-Jenson et al. [42] show that winding deformation, displacement, short circuit and change in oil permittivity alter the transfer function. Malewski et al. [43] reported that the transfer function could identify faults from resonant frequency shifts and resonant pole damping. They have also reported that the transfer function method is sensitive to the differences between local breakdowns and partial discharges in the winding insulation. This is an important property as the former disqualify the transformer whereas the later can be tolerated since discharge free behaviour of the winding insulation is not a requirement at the BIL. Other results show that the

transfer function changes with ground leakage.

The transfer function method is a very attractive transformer insulation evaluation tool, as the resulting transfer function is independent of the test waveform. Thus, malfunctions of the impulse generator or scatter in the chopping time do not affect the comparison of transfer functions. Therefore the transfer function method, by its very nature, avoids the first two limitations of the conventional technique given in the last section. Further, the transfer function method allows a comparison of the transadmittance functions obtained by the application of full and chopped impulses.

Batruni et al. [61] have suggested that the transadmittance function can be used to detect thermal aging. They arrived at this conclusion by evaluating the affect of accelerated thermal aging tests on the capacitance and conductance of oil impregnated paper insulation, and substituting the results into a lumped parameter winding model. Although further work needs to be done in this area their findings are encouraging. Bak-Jenson et al. [42] have performed accelerated aging tests by short circuiting windings and applying overvoltages on a cyclic basis to determine whether it is possible to identify a development in the transfer function towards breakdown of the transformer. Findings suggest that detection can only be achieved if the degradation causes changes in the winding capacitance, total losses or reluctance. Furthermore two failures that produce an equivalent effect, such as raising the effective magnetising losses, are inseparable with the transfer function method.

3.5.1 On-Line Monitoring using the Transfer Function

The transfer function method can also be used for on-line monitoring of transformers in power systems. Recently Leibfried and Feser [40] have been looking at the prospect of using system generated transients and disturbances as the source of excitation for determining the transfer function. However, these signals must have adequate spectral characteristics if the transfer function is to be determined to a high enough frequency to ensure reliable fault detection.

The use of system generated and natural transients and disturbances poses the following problems and difficulties:

- Surge arrestors are used in power systems to divert potentially harmful transients. Using these transients as an excitation source exposes the transformer's insulation to additional stresses that may affect the service life of the transformer.
- The frequency of occurrence of transients with adequate spectral characteristics may

mean that the required transfer function is determined on an infrequent basis.

- Complex data acquisition hardware needs to be designed due to the unknown parameters of the signals to be digitised viz. the peak voltage and time duration.
- Leibfried and Feser [40] have suggested that a digitiser with sampling rate of 10MHz and time record duration of 10ms is needed to completely acquire system generated transients. Such a system generates an enormous amount of data that requires powerful hardware for processing in real-time. Furthermore, multirate digital signal processing complexities are introduced if a switchable sampling rate is used.

Leibfried and Feser [40] have demonstrated that inductive and capacitive coupling between phases in a three phase system due to switching operations etc., cause the superposition of high frequency oscillations onto the signals being digitised. If the digitiser has insufficient memory to record these oscillations, then the resulting truncation introduces errors into the transfer function calculations. The system described in [40] high pass filters the recorded transient data to reduce the time duration in order to avoid these errors.

Additional difficulties associated with determining the transfer function on-line, either through the use of system generated transients or via supplied excitation, include:

- The power system components surrounding a transformer can have an affect on the transfer function calculated across a transformer. This is because the signal measured at the LV winding may have a load reflection component superimposed. As a result the transfer function may be affected by changing system configurations. Further research needs to be performed in this field to differentiate system configuration transfer function changes from internal faults.
- In 7.3 it is shown that temperature affects the calculated transfer function. Because a transformer's internal temperature is function of it's loading, then the transfer function also becomes a function of a transformers loading. Again, further research needs to be performed to distinguish these changes from internal faults.
- The influence of the position of transformer tap changers also needs to be studied.
- Transformer core magnetization changes throughout a 50Hz cycle cause self and mutual inductances within a winding to vary on a cyclic basis. As a result, at higher frequencies, the measured transfer function may be affected by the time difference between a 50Hz zero crossing and the recording of transient data. Section 7.4.1 discusses synchronising tests to the 50Hz supply cycle and presents the results obtained by testing a 7.5kVA single phase distribution transformer.

3.6 On-Line Diagnosis

In a multi-sensor environment, a step toward a fully automated on-line diagnostic system would be to appropriately process the information received from all sensors, in order to provide the power system engineer with information-rich diagnostic messages. Diagnosis would be most effective if several levels of analysis were performed. A potential system would need both a fast response, to avoid catastrophic failure of the transformer, as well as detailed, time-intensive levels of analysis. A possible system may include the following analysis steps

- **System check:** When a severe or rapidly developing anomaly or problem occurs the fastest response will be required. A decision will need to made as the whether the transformer needs to be shutdown or can be left on-line. Because of the costs involved with transformer shutdown, fast checks based on Built-In Test Equipment (BITE) tests may first be done to verify that there is not a sensor problem. Some anomalies may not be determinable, indicating the need to invoke human intervention.

- **Correlation check:** When a problem develops more slowly, more analysis will take place over a longer period of time. The correlation check will be concerned with correlating results from different sensors, in order to make a more accurate diagnosis. To give even more accuracy, this level of diagnosis will have access to off-line and periodic test results (e.g. DGA tests) for the transformer.

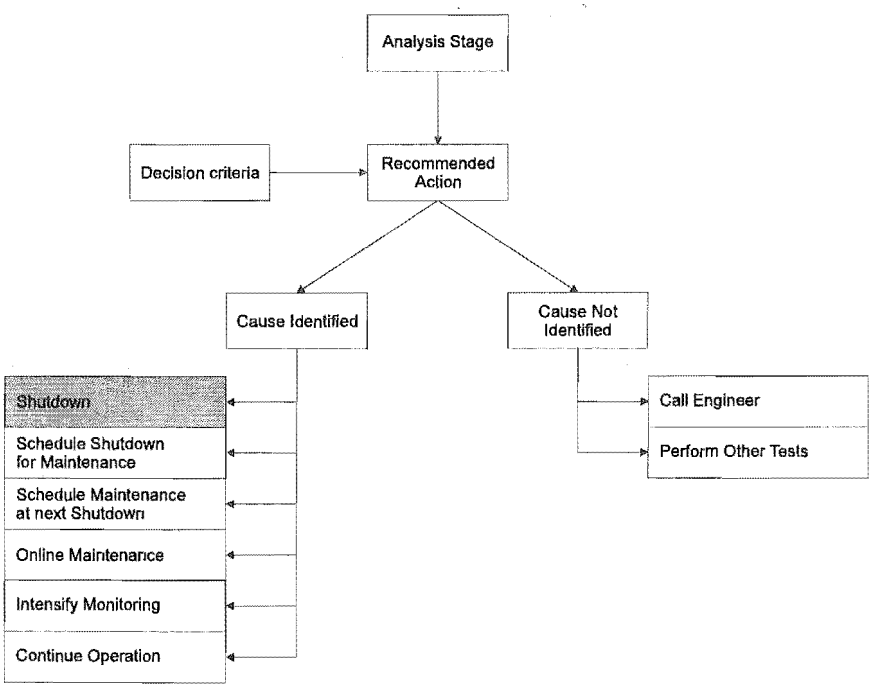

Figure 3.2 Decision making following analysis

- **Statistical trending and database comparison:** The most slowly developing anomaly or problem may require the preceding analysis stages, and in addition statistical trending and database comparison. This will allow a more detailed analysis of all the information available, including that residing in external databases, such as parameter trending for the class of transformer.

If the system can identify the cause of the anomaly or problem with some certainty, a recommended action based on some set decision criteria can be made to the power system engineer. The decision making illustrated in Figure 3.2 may follow each analysis stage.

In support of the ideas presented in this section, recent publications have indicated the following technical trends:

- The application of artificial intelligence systems for interpreting sensor outputs
- Development of on-line diagnostic techniques
- A shift from on-line monitoring and off-line diagnostics to on-line diagnostics

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Chapter 4

HARDWARE DESIGN

The purpose of this chapter is to describe the hardware design of the TICMS prototype. The first section gives an overview of the design and identifies the main modules. Section two describes the impulse generator module (IGM) used to excite the transformer while section three presents the design of the transducers used to interface the transformer to the data acquisition and processing module (DAPM). The buffers and transmission lines used to connect the IGM to the DAPM are discussed in section four while the design of the DAPM and each of its components are presented in the remaining sections.

4.1 Overview

The TICMS consists of two instruments and an attached PC and is connected to a transformer as shown in Figure 4.1. The first instrument is a low voltage IGM (Impulse Generator Module) that provides the excitation needed to determine the transadmittance function. The second instrument is a high speed DAPM (Data Acquisition and Processing Module) that digitises the input impulse along with the response from the transformer so that digital signal processing can be used to determine the winding transadmittance function. Transducer circuitry is also used to interface the system to the transformer and to attenuate the signals down to a level that is compatible with the DAPM. The transducer circuitry is housed in the IGM enclosure.

A high speed serial link is used to attach the DAPM to the PC. The PC is used to issue commands to the DAPM and receives captured and processed data in response. This is then displayed graphically for user interpretation. A control line between the DAPM and the IGM allows test procedures to be automated.

An additional instrument (not shown in Figure 4.1) called the Test Synchroniser Module (TSM), is used when the TICMS performs on-line testing. The TSM is used to synchronise the test instant to a point in the 50Hz cycle of the supply to the TUT. Further details relating

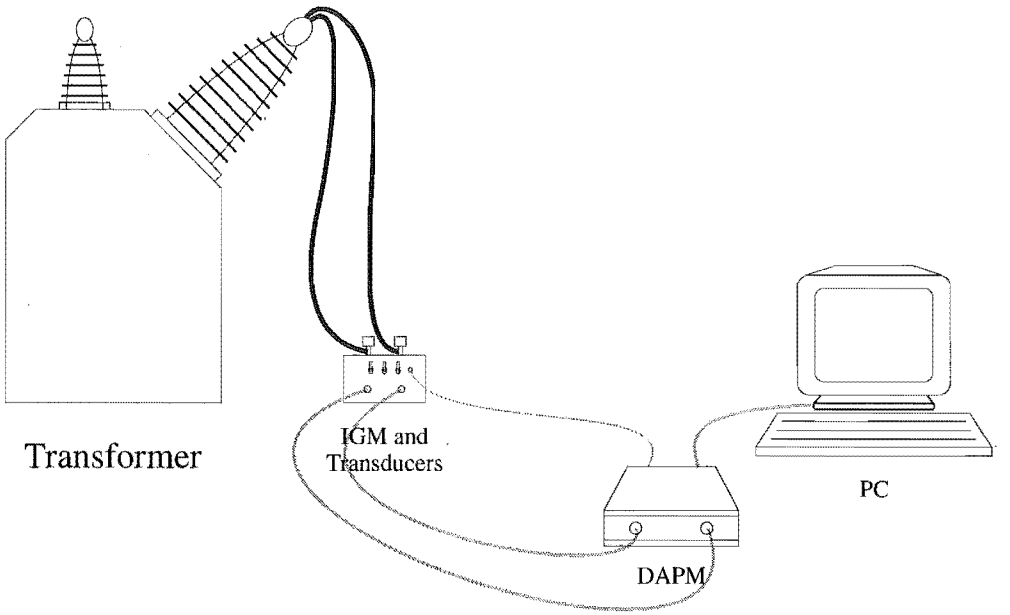

Figure 4.1 The Transformer Insulation Condition Monitoring System

to this technique are given in 4.3.

4.2 Impulse Generator Module

The IGM consists of a single stage impulse generator circuit and control circuitry as shown in Figure 4.2. To generate an impulse first capacitor C_1 is charged to the DC supply voltage by closing switch S_1. Next S_1 is opened and S_2 closed causing the charge on C_1 to pass through the waveshaping network made up of R_1, R_2 and C_2 so that an impulse is produced at the output. The control circuitry is responsible for opening and closing the switches at the correct times. A control input from the DAPM can activate the control circuitry causing an impulse to be generated.

The waveshape of the impulse is determined by the RC values used in Figure 4.2. To a first approximation R_1 determines the front time as it limits how fast C_2 can be charged while R_2

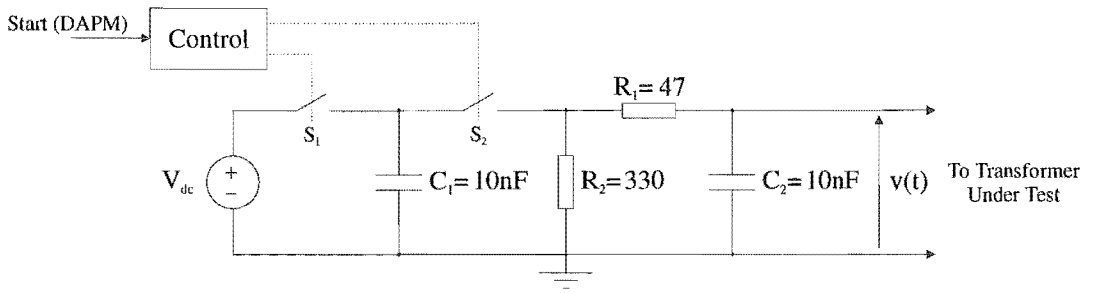

Figure 4.2 Impulse Generator Module

discharges both capacitors and therefore essentially controls the wavetail. A detailed analysis of the circuit is given in Appendix D where it is shown that the waveshape of the impulse is given by

$$v(t) = \frac{V_{dc}}{R_1 C_2(\alpha_2 - \alpha_1)}\left[e^{-\alpha_1 t} - e^{-\alpha_2 t}\right] \tag{4.1}$$

where

$$\alpha_1, \alpha_2 = \frac{1}{2}\left(\frac{1}{R_1 C_1} + \frac{1}{R_1 C_2} + \frac{1}{R_2 C_1}\right) \mp \sqrt{\frac{1}{4}\left(\frac{1}{R_1 C_1} + \frac{1}{R_1 C_2} + \frac{1}{R_2 C_1}\right)^2 - \frac{1}{R_1 R_2 C_1 C_2}} \tag{4.2}$$

The waveform produced by the impulse generator circuit in Figure 4.2 is shown in Figure 4.3. For an impulse the 'wavefront' is defined as 1.25 times the time interval between points on the wavefront at 10% and 90% of it's peak, whereas the 'wavetail' is defined to be the total time taken for the impulse to rise to it's peak value and then fall to half peak. Based on these definitions, the impulse produced by the IGM in Figure 4.3 has a wavefront of 0.5μs and a wavetail of 5.8μs. The actual waveshape produced by the IGM differs a little from

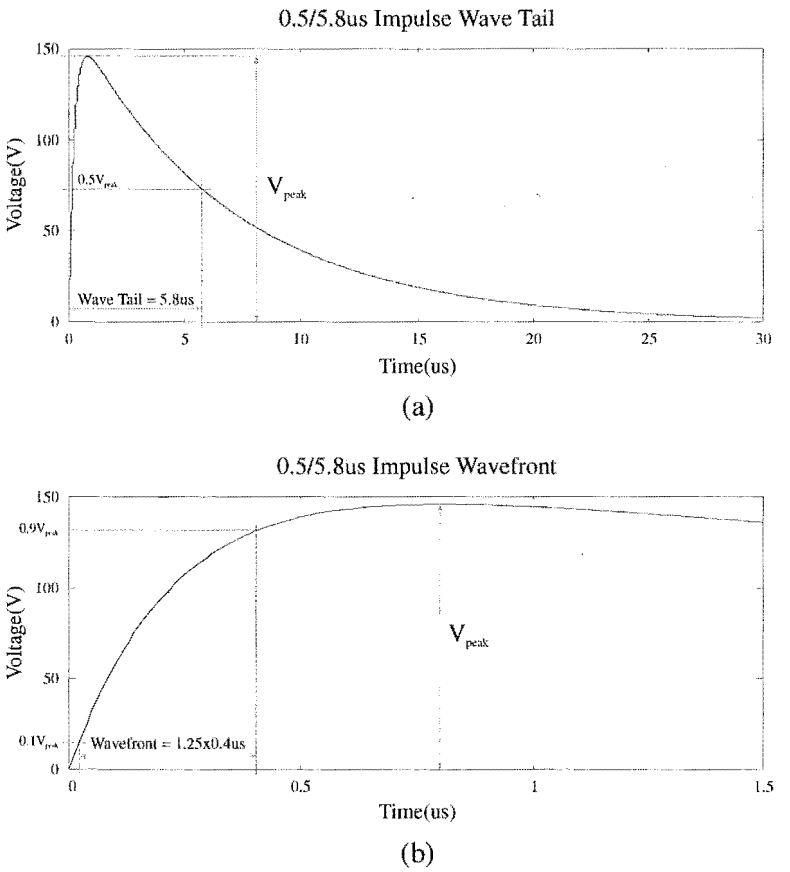

Figure 4.3 IGM 0.5/5.8μs impulse waveshape. (a) Wave Tail (b) Wavefront

that in Figure 4.3 due to the affects of the voltage transducer and transformer loading.

Rectified mains supplied via an isolated variac is used as the source of DC in Figure 4.2. The variac allows the peak voltage of the impulse to be controlled. With the variac set at maximum, the efficiency of the RC implementation determines the maximum peak impulse voltage that the IGM is capable of producing. The efficiency is derived in Appendix D and is equal to

$$\eta = \frac{V_{peak}}{V_{dc}} = \frac{(\alpha_2/\alpha_1)^{-\alpha_1/(\alpha_2-\alpha_1)} - (\alpha_2/\alpha_1)^{-\alpha_2/(\alpha_2-\alpha_1)}}{R_1 C_2(\alpha_2-\alpha_1)} \tag{4.3}$$

Substituting α_1 and α_2 from Eq. (4.2) into Eq. (4.3) results in an efficiency of 43% when the RC values in Figure 4.2 are used. This allows the IGM to produce an impulse with a variable peak voltage up to a maximum of

$$V_{peak} = V_{dc} \cdot \eta = 240 \cdot \sqrt{2} \cdot 0.43 = 146V \tag{4.4}$$

as illustrated in Figure 4.3. The efficiency can be increased by adjusting the RC values in Figure 4.2 but this affects other characteristics of the generated impulse. In summary the values used are a trade-off among the following characteristics

- **Waveshape:** The waveshape is used to control wavefront and wavetail times in order to tailor the spectral characteristics of the transformer excitation.
- **Efficiency:** The efficiency is used to control the maximum peak voltage that can be produced.
- **Output impedance:** The output impedance is used to control the affect of voltage transducer and transformer loading.
- **Current transient peak:** The peak magnitude of the current transients that result when the switches in Figure 4.2 are closed determines electronic switch rating requirements.

4.2.1 Control Circuitry

The control circuitry illustrated in Figure 4.4 is used to generate non overlapping active high pulses to turn on S_1 and S_2 in Figure 4.2. Pulse transformers are used to isolate the control circuitry from the impulse generator circuit. More detailed IGM schematics can be found in Appendix J.

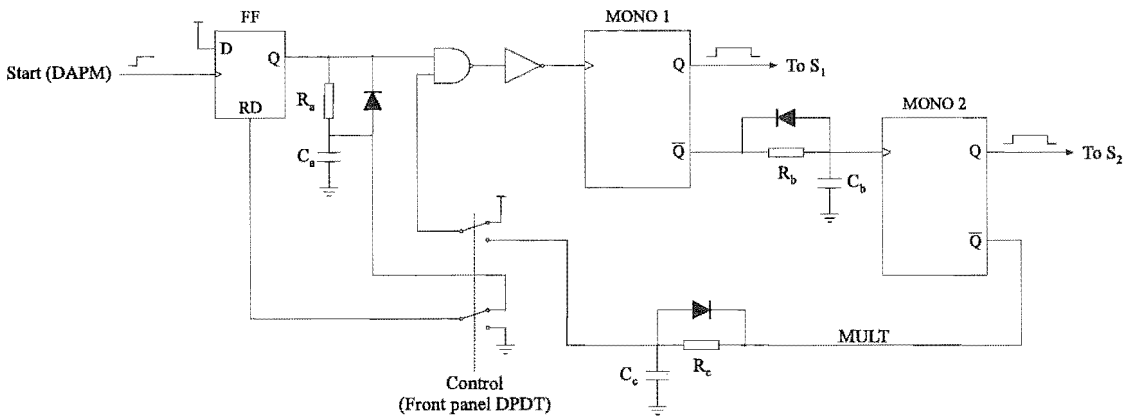

Figure 4.4 IGM control logic

The control circuitry can place the IGM in one of two operational modes. The single mode allows a single impulse to be generated upon the receipt of a control signal from the DAPM while the multiple mode allows a train of impulses to be produced. The operational mode is selected by a DPDT switch on the front panel of the IGM.

When the DPDT switch in Figure 4.4 is in the up position the IGM is in single mode. When in single mode the control signal from the DAPM activates a flip-flop that activates the MONO 1 monostable which generates the pulse used to turn on S_1. R_b and C_b are used to delay the rising edge of the inverted output of MONO 1. This delayed edge activates MONO 2 which generates the pulse used to turn on S_2. The delay ensures that the pulses to S_1 and S_2 are non-overlapping so that both switches are never on at the same time. The timing of these events is illustrated in Figure 4.5.

When the DPDT switch is in the down position the IGM is in multiple mode. Multiple mode differs from single mode operation in that the inverted output of MONO 2 is used to

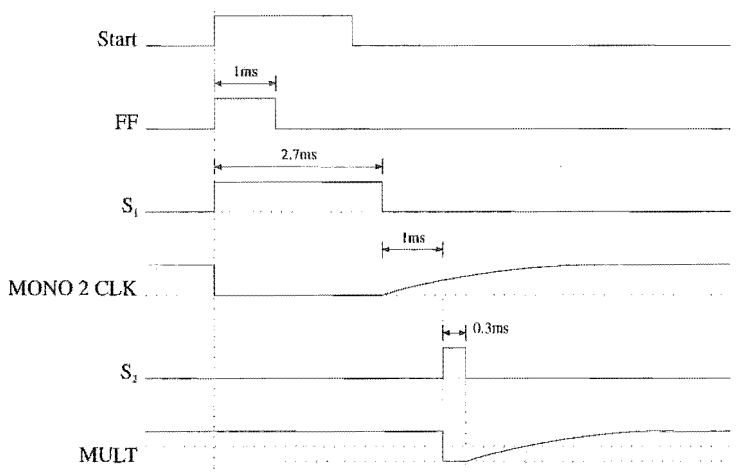

Figure 4.5 IGM control timing

reactivate MONO 1. This causes the timing cycle to repeat so that an impulse train is produced. R_c and C_c are used to delay the rising edge of the inverted output of MONO 2 which allows the time between consecutive impulses to be controlled. To leave the multiple mode the DPDT switch is moved to the up position so that the flip-flop can reset which prevents MULT from initiating another cycle. An alternative way to generate an impulse train is to have the DAPM send multiple strobes to the IGM. The DAPM application software is used to send these strobes to the IGM as the software can easily produce the timing required to generate an impulse train for many different testing procedures. The DAPM application software is discussed in greater depth in 6.2.

Each RC combination in Figure 4.4 introduces a delay of $RC\log_e 2$ as the CMOS logic used has a switching threshold of half the rail voltage. The RC values used give rise to the timing in Figure 4.5. The resulting pulse widths exceed the minimum values required for the impulse generator circuit to function properly.

Finally the user can cause the IGM to generate an impulse by manually activating the momentary switch on the front panel. This allows preliminary tests to be performed on a new transformer without the DAPM connected so that the analog waveforms can be appropriately attenuated for the DAPM.

4.3 Test Synchroniser Module

The TSM is a separate instrument that is used to synchronise the application of an impulse from the IGM to a point in the 50Hz cycle of the supply to the TUT. This allows test sets to be conducted that can evaluate the effect of core magnetisation on the transadmittance function. Further details and experimental results can be found in 7.4.1.

The TSM is only used during on-line test sequences where it is connected between the DAPM and the IGM. After being activated by a control voltage from the DAPM, it activates the input of the IGM control circuitry the next time the TUT supply voltage passes through a given point in the 50Hz cycle. The TSM is shown in Figure 4.6 and consists of the following components:

- **Transformer and comparator:** The comparator produces a positive edge everytime the supply voltage of the TUT exceeds an adjustable DC level. The DC level is controlled by a multi-turn pot. The peak-to-peak value of the TSM transformer secondary voltage is equal to Vcc.
- **Flip-flop:** The flip-flop output drives the input of the IGM control circuitry. After the

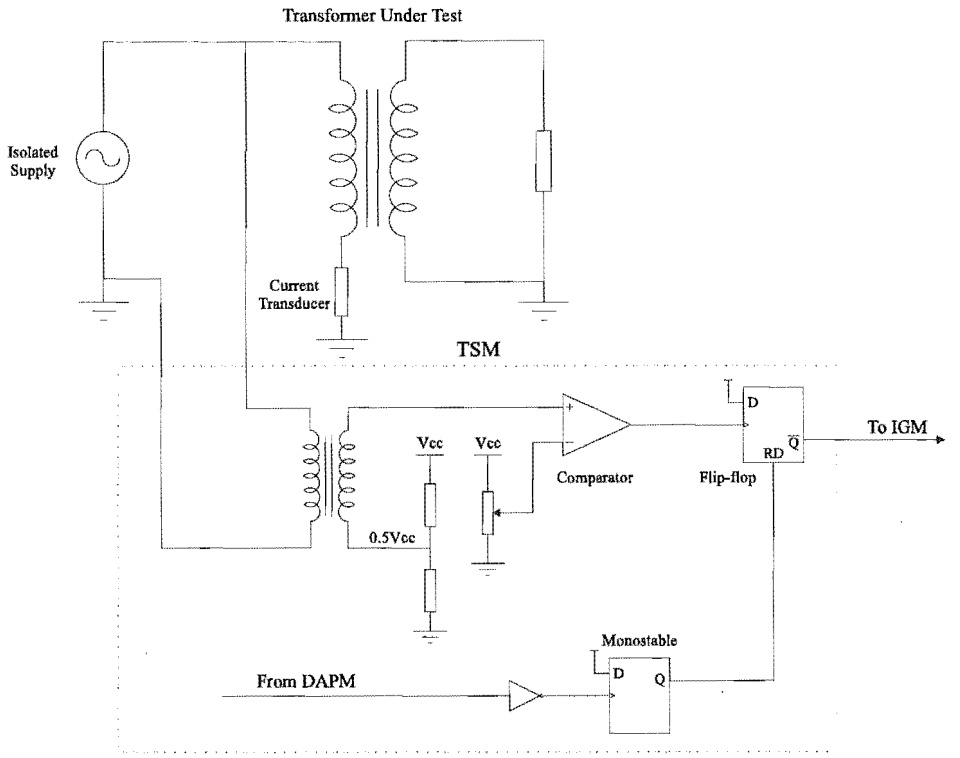

Figure 4.6 The TSM and it's interface

flip-flop has been reset, the next positive edge from the comparator sets it, which causes the IGM to generate an impulse. The flip-flop remains set until the next test request is made.

- **Inverter and monostable:** A test request produces a negative edge on the control line at the output of the DAPM. After being inverted by a BJT inverter, this activates a monostable which resets the above flip-flip.

The pot in Figure 4.6 is used to control the point in the 50Hz cycle to which the tests are synchronised. With the pot adjusted as far as it can go clockwise, an impulse is produced by the IGM 0.32ms from a positive going zero crossing. Table 4-1 lists the synchronisation times (time from positive going zero-crossing) each time the pot is turned one full turn anti-clockwise. The synchronisation times were measured using a digital storage oscilloscope, by recording the amplitude of the AC supply at the instant that the impulse was produced. Because the AC supply in the EEE Department has a flat top, the last five synchronisation times could not be determined accurately. The flat top is primarily due to the large number of PCs in the department, all of which draw current from the supply near the peak of the cycle. In summary adjusting the pot across it's entire range shifts the synchronisation time over a ¼ of a cycle, from just above a positive going zero-crossing to the negative trough.

Anti-clockwise turns	Synchronisation time	Anti-clockwise turns	Synchronisation time
0	0.32 ms	7	-3.57 ms
1	-0.32 ms	8	-4.28 ms
2	-0.8 ms	9	-5 ms
3	-1.33 ms	10	-5 ms
4	-1.83 ms	11	-5 ms
5	-2.27 ms	12	-5 ms
6	-2.9 ms	13	-5 ms

Table 4-1 TSM test synchronisation times

4.4 Transducers

Transducers are used to interface the transformer to the DAPM and to attenuate analog signals down to a level compatible with the DAPM. Their design allows the effective dynamic range of the DAPM to be extended, and on-line testing to be performed. The transducers used must have a bandwidth of at least 3MHz if they are to introduce no distortions into the transadmittance function over the bandwidth of interest.

4.4.1 Voltage Channel Transducer

The voltage channel transducer consists of an RC high pass filter as shown in Figure 4.7. The filter attenuates the large magnitude low frequency components of the input impulse, causing the effective number of bits for the digitisation process to be increased. This concept is illustrated in Figure 4.8. The DAPM application software makes such an increase possible by restoring attenuated components that are below the filter cutoff. This is achieved by dividing the spectra of the digitised signal by the transfer function of the voltage transducer, as discussed in 5.6. This scheme is possible as the 1st order roll-off of the filter results in attenuated components that are still above the quantisation noise floor introduced by the digitiser. As a result of the increase in effective dynamic range, the transadmittance function can be determined over a wider frequency range.

The voltage divider made from R_1 and R_2 in Figure 4.7 provides amplitude control and is used to ensure that the filtered impulse occupies the full scale input voltage range of the DAPM. This maximizes the SNR during the digitisation process as discussed in 5.2.2. To prevent the cutoff frequency from changing when adjusting R_1 and R_2 it is necessary to keep

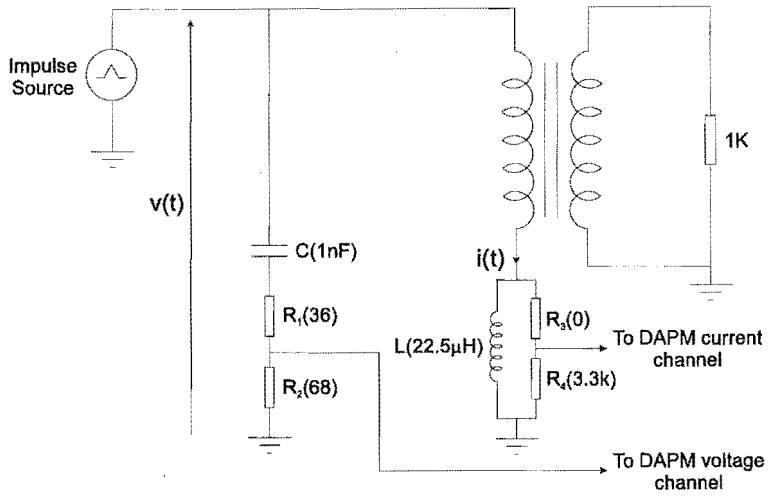

Figure 4.7 Voltage and current transducers

their sum constant.

In Appendix E it is shown that the magnitude spectrum of the filter transfer function is

$$\text{Gain(dB)} = 20\log_{10}\frac{\omega}{\omega_2} - 20\log_{10}\sqrt{1+\left(\frac{\omega}{\omega_{12}}\right)^2} \tag{4.5}$$

where

$$\omega_2 = \frac{1}{R_2C},\ \omega_{12} = \frac{1}{(R_1+R_2)C} \tag{4.6}$$

The cutoff frequency of the filter in Figure 4.7 is

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi(36+68)(1e^{-9})} = 1.53\text{MHz} \tag{4.7}$$

thus providing

$$-\left(20\log_{10}\left(\frac{50}{1.53e^6}\right) - 20\log_{10}\sqrt{1+\left(\frac{50}{1.53e^6}\right)^2}\right) = 90\text{dB} \tag{4.8}$$

of attenuation at 50Hz. Therefore the voltage transducer design also prevents the sinusoidal input to the transformer from taking up dynamic range when the TICMS is being used to determine the transadmittance function for a transformer in service. The 50Hz power signal shown in Figure 4.8 takes up dynamic range during online testing when the voltage channel transducer is not used.

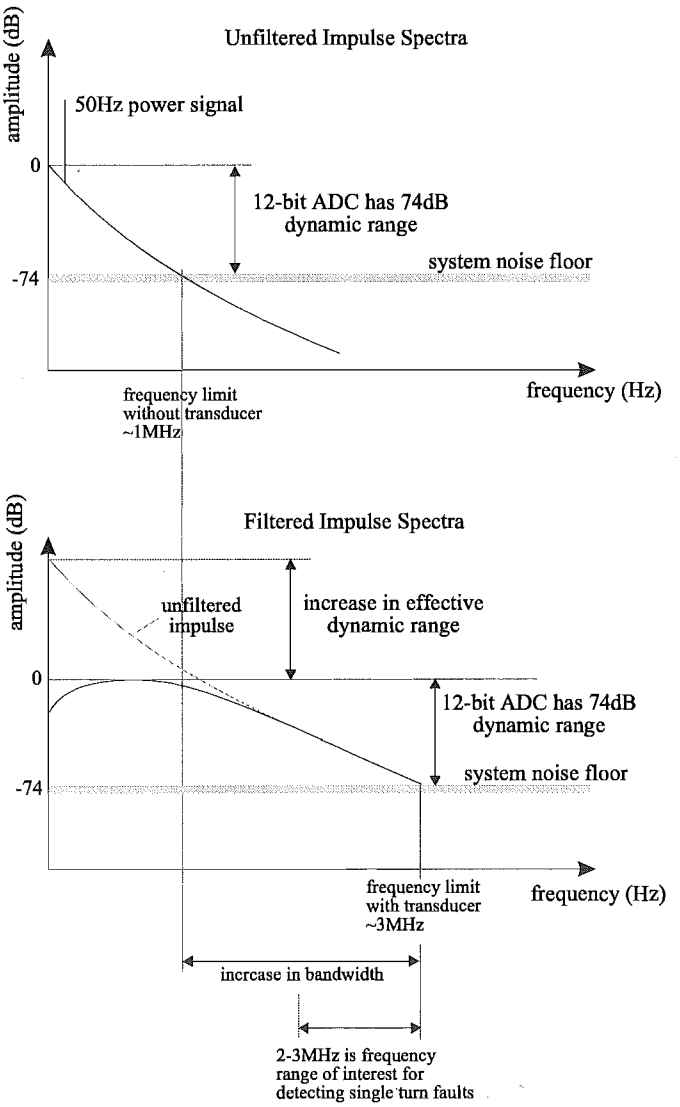

Figure 4.8 Increasing the effective dynamic range

4.4.2 Current Channel Transducer

An RL shunt is used for the current channel transducer as shown in Figure 4.7. Because the reactance of the shunt increases with frequency, the higher frequency current components produce a larger voltage drop across the shunt than lower frequency ones of the same magnitude. Hence the shunt acts similarly to the RC filter on the voltage channel in that it promotes the small magnitude high frequency components at the expense of the low frequency ones.

In Appendix E it is shown that the transfer function of the shunt is equal to

$$H(j\omega) = \frac{j\omega R_4/\omega_c}{1+j\omega/\omega_c} \qquad (4.9)$$

where

$$\omega_c = \frac{R_3+R_4}{L} \tag{4.10}$$

The DAPM application software uses Eq. (4.9) to calculate the current through the TUT as discussed in 5.6. Like the voltage transducer, the shunt resistors R_3 and R_4 provide amplitude control, allowing the data acquisition system to be optimised without affecting the current transducer frequency response.

The 50Hz reactance of the shunt in Figure 4.7 is

$$\frac{\omega L(R_3+R_4)}{\omega L+R_3+R_4} = \frac{\left(2\pi\cdot 50\cdot 22.5e^{-6}\cdot 3.3e^{3}\right)}{2\pi\cdot 50\cdot 22.5e^{-6}+3.3e^{3}} = 7.1m\Omega \tag{4.11}$$

Because the TICMS has been designed to monitor the insulation condition of the HV winding of a transformer, lower primary currents are encountered and as a result little voltage drop is produced across the shunt at 50Hz. This allows the shunt to be used to determine the transadmittance function of a transformer in service as it's neutral terminal is essentially kept at ground potential at 50Hz.

4.5 Buffers and Coaxial Lines

The signals from the voltage and current transducers in Figure 4.7 are buffered prior to being connected to the DAPM. A BJT push-pull follower with a 10Ω output impedance is used for each buffer. The low output impedance prevents an excessive increase in the source impedance of the signals being digitised after additional attenuation by the DAPM. As the BJTs in each buffer are connected in a common collector configuration then each buffer has a bandwidth in excess of 5MHz. This is sufficient to ensure that no distortions are introduced into the transadmittance function up to 3MHz. Hardware schematics of the buffers can be found in Appendix J.

Each buffer drives a 50Ω coaxial line that connects to the DAPM. Because the coaxial lines are terminated with 50Ω at the DAPM, each signal source sees a pure 50Ω resistance at all frequencies. This prevents the coaxial line capacitance (typically 100pF per meter) from affecting the transadmittance function. Failing to treat each coaxial line as a transmission line makes the transadmittance function dependent upon line capacitance, and therefore line length. Further, the temperature coefficient of line capacitance would result in transadmittance function changes with temperature, clearly undesirable.

Assuming the maximum frequency of interest to be the Nyquist frequency we find that the smallest wavelength encountered is

$$\lambda = \frac{\frac{2}{3}c}{f_{\frac{1}{2}}} = \frac{2{\cdot}3e^{8}}{3{\cdot}5e^{6}} = 40m \qquad (4.12)$$

where the speed of electromagnetic wave propagation has been taken as 2/3 of the speed of light, a figure typically used in transmission line calculations. For the current laboratory setup the length of each coaxial line is 1.5m, making the line length much less than the smallest wavelength encountered. As a result transmission line effects are not noticeable. Because each coaxial line has been terminated in an impedance equal to it's characteristic impedance, the line length can be increased as needed to locate the DAPM remotely from the TUT without fear of introducing measurement errors into the system due to voltage reflections at the DAPM.

4.6 Data Acquisition and Processing Module

A functional block diagram of the DAPM is illustrated in Figure 4.9. The DAPM contains a voltage channel and a current channel that digitise and process the voltage and current analog transients that result from an insulation test. The design of the DAPM can be divided into the following

1. Analog Signal Conditioning
2. Transient Digitiser (TD)
3. Digital Signal Processor (DSP)
4. Memory Interface
5. UART Interface
6. FPGA Design
7. Power Supply

The design of each of these components is discussed in the sections to follow.

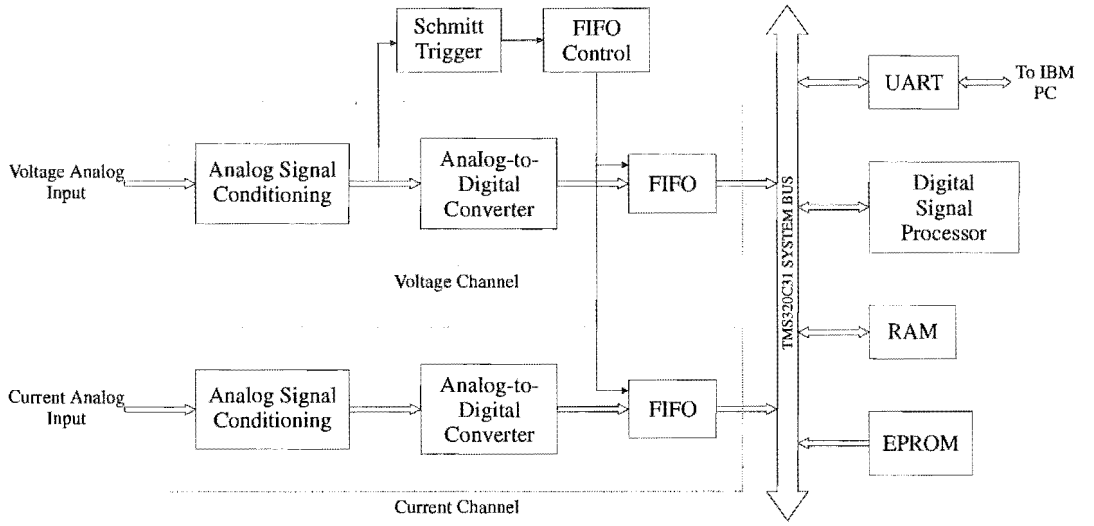

Figure 4.9 DAPM Block Diagram

4.7 Analog Signal Conditioning

Analog signal conditioning is used to get the analog transients into a form that maximises the SNR during the digitisation process. A block diagram of the analog stages used is pictured in Figure 4.10.

Resistive voltage dividers are used to attenuate the signals that arrive at the DAPM down to 3V, making them compatible with the op amp stages to follow. The first op amp stage buffers the signals, reducing their source impedance for the op amp stage to follow. The second op amp stage subtracts a DC voltage from each analog transient so that the bipolar input voltage range of each analog-to-digital converter is utilized. This is necessary in order to prevent the loss of a bit when digitising a unipolar signal (each analog-to-digital converter has an input voltage range -1V to 1V). The loss of a bit of vertical resolution raises the quantisation noise floor by 6dB, reducing the frequency to which the transadmittance function can be determined to as discussed in 5.3. Trimming pots are available to adjust the DC voltage subtracted so that the system can be easily optimised for

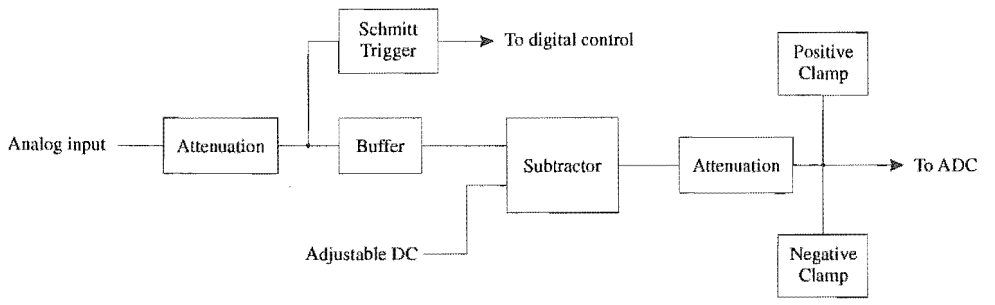

Figure 4.10 Analog signal conditioning for one channel

future tests setups. For the present test setup no DC voltage needs to be subtracted in the current channel as the waveform from the RL shunt is almost symmetrically bipolar as shown in Figure 6.5b). The voltage channel signal shown in Figure 6.5b), is close to being unipolar and therefore requires that a DC voltage be subtracted if it is to be attenuated to occupy -1V to 1V.

A schmitt trigger is used on the voltage channel only, to signal to the digital control circuitry whenever the analog input voltage exceeds a predetermined threshold. This allows the DAPM to detect when a test is in process and issue the necessary control signals to the TD for successful data acquisition.

A resistive voltage divider on each channel attenuates the signals down to the -1V to 1V range, just prior to digitisation. Keeping the analog signals as large as possible for as long as possible minimises the affect of analog noise, maximising the SNR.

Protection is used prior to each analog-to-digital converter, as the devices used in the DAPM design are expensive. Clamping circuits are used to implement the protection. The clamps provide protection against excessive positive and negative voltages at the analog input of each converter.

4.8 Transient Digitiser

The TD digitises the transient signals resulting from a transformer insulation test, making the resulting data available to the DSP for processing. The TD consists of an analog-to-digital converter, a high speed first-in-first-out (FIFO) memory buffer and interface logic on each channel of the DAPM. Figure 4.11 illustrates the TD components for one DAPM channel. All interface and control logic is implemented in an FPGA.

4.8.1 Analog-to-Digital Converters

The analog-to-digital converters (ADCs) are one of the most important components in the TICMS design as they are one of the major sources of error and therefore limit the overall performance of the system. Selection of the right ADC is therefore critical if the TICMS is to perform as required. A 12-bit two-step subranging ADC is used on each DAPM channel. The converters used have a maximum sampling rate of 10MHz and convert the sampled data to 12-bit 2s complement format. Synchronous sampling on each channel is achieved by driving each ADC with the same sampling clock signal.

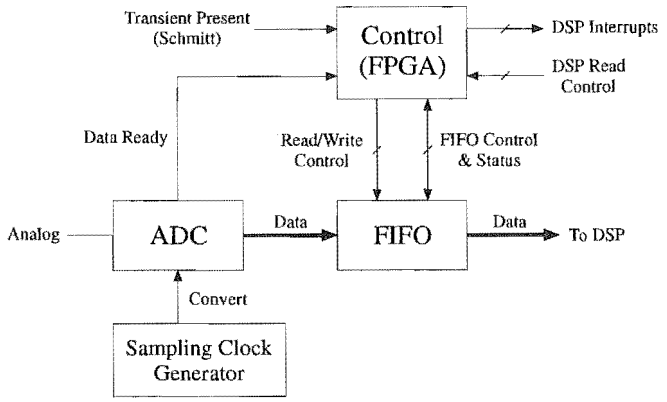

Figure 4.11 TD components for one channel

The analog input voltage range of each ADC is from -1 to 1V. The 2V range results in an LSB of

$$\text{LSB} = \frac{2}{2^{12}} \approx 0.5\text{mV} \tag{4.13}$$

Therefore increasing the analog input voltage by 0.5mV causes the ADC digital output to increment by 1. It is difficult to try and keep analog noise below this voltage, especially in a high speed mixed signal system. For the TICMS design analog noise degrades the ENOBs of each ADC to 9. Further discussion on the ENOBs is presented in 5.2.3 while 6.3.5 introduces the DAPM software diagnostic test used to measure the ENOBs.

The ADC sampling rate of 10MHz ensures that no aliasing occurs, provided that no signal components beyond 5MHz are above the system noise floor. An excitation with these spectral characteristics was used in the TICMS design, as discussed in 5.2.5. Excess sampling rate is used to ensure that aliasing does not result should transformer resonances cause current components beyond 3MHz to appear above the noise floor. Aliasing issues are further discussed in 5.2.4.

The digital output from each ADC is in 12-bit 2s complement format. Before processing can begin, the DAPM applications software changes the data format to 32-bit signed integer format, and then to 32-bit TI floating point format. After the processing is complete the data format is converted to single precision IEEE floating point format so that it can be sent to a PC. See Appendix A for further details on the data format conversion.

4.8.2 FIFO Memories

FIFO memory devices are needed as rate buffers on each DAPM channel as the maximum I/O data transfer rate of the DSP is 5.55Mwords/s. This rate is achieved when using the DSP's on-chip DMA controller to perform the transfer and is insufficient to keep up with

the 10Mwords/s data transfer rate from the ADCs.

Each FIFO can hold 1024 words of data when full and has output flags that indicate when the device is full, half full, empty and contains more than X words where X is programmable. The DAPM uses these flags to control the state of the TD. The different states that the TD can be in at one time are shown in Figure 4.12 where the shaded sections indicate the locations that contain valid data. Each of the states is now briefly discussed.

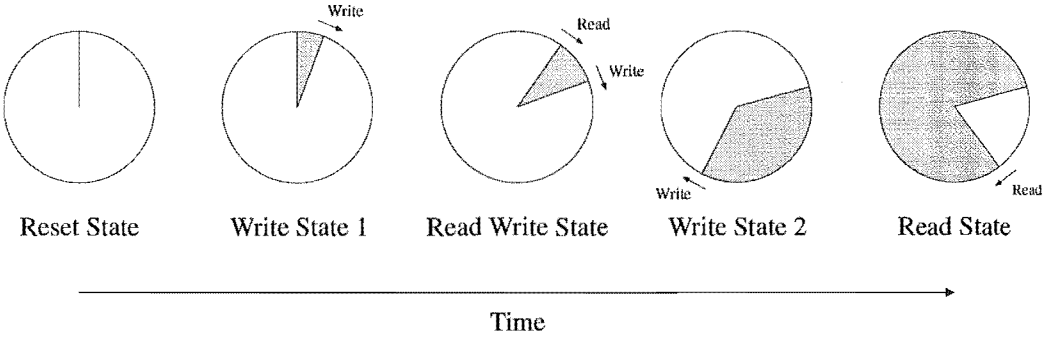

Figure 4.12 TD States

4.8.2.1 Reset State

The reset state is needed to put all TD interface logic and both FIFOs into a known state. The TD is reset at power up and after data has been acquired for a transadmittance function test. Therefore after each test, the TD is rearmed, ready for the next acquisition. The hardware and timing for the reset state are shown in Figure 4.13 and Figure 4.14 respectively.

The TD is placed into the reset state when software causes the DSP to produce a logic 0 pulse on its $\overline{\text{IACK}}$ output pin. This causes the transient digitizer reset pulse generator (TDRPG) shown in Figure 4.13, to produce a pulse that resets all flip-flops and both FIFOs.

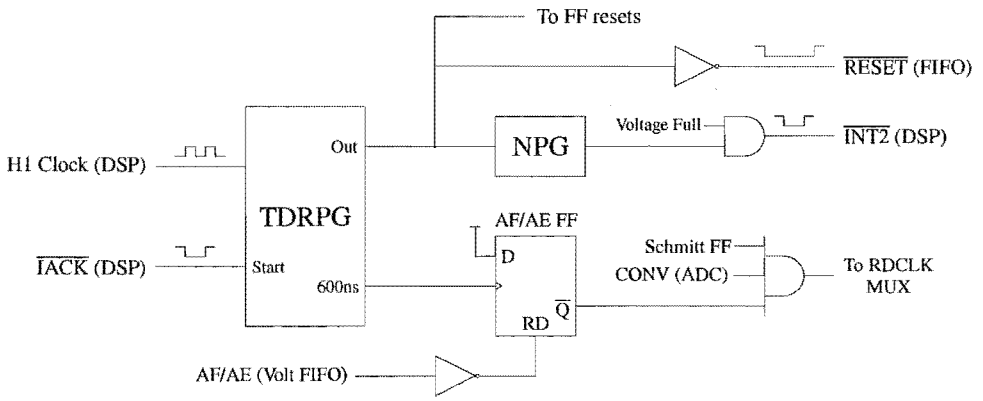

Figure 4.13 TD reset logic

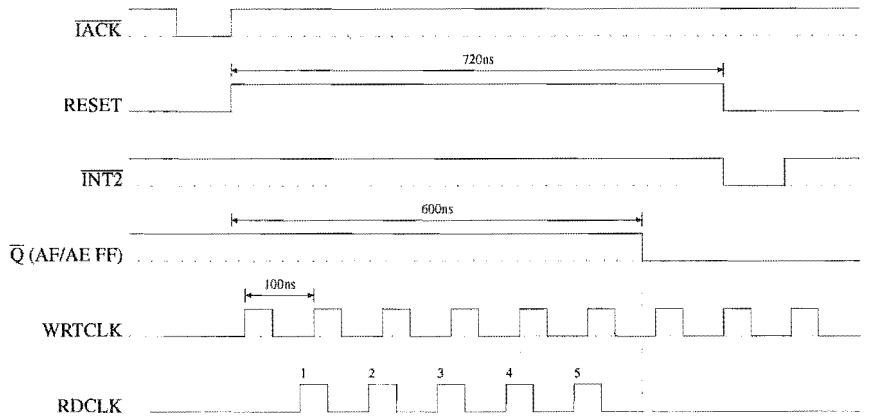

Figure 4.14 Reset state timing

At the end of the TDRPG pulse the negative-edge pulse generator (NPG) generates an interrupt to the DSP, informing the application software that the TD has been successfully reset and is ready to capture more data. Because the voltage FIFO has just been reset, the Voltage Full signal is high and the NPG pulse is not prevented from interrupting the DSP.

For the FIFOs to be reset correctly it is necessary that each see a minimum of four read and write clock strobes during the reset state. As these strobes come from the data ready and convert strobes of the ADCs every 100ns then this requirement is satisfied as the reset state is 720ns long (see Figure 4.14). Before leaving the reset state the read clock strobes must be gated off from each FIFO, to allow the TD to enter the next state. This is achieved by resetting the AF/AE flip-flop 600ns into the reset state, long enough to ensure that at least four read clock strobes have passed under worst case timing conditions. This delay takes into consideration that the strobes from the ADCs are asynchronous to the TDRPG reset pulse.

The read strobes in Figure 4.13 are passed to the RDCLK MUX. The RDCLK MUX is used to select the read strobe source. ADC read strobes are used when the TD enters the read-write state. DSP read strobes are used during the read state, when data is being acquired for processing. Read-write and read state discussions follow. The Schmitt FF signal in Figure 4.13 allows the ADC read strobes to be gated off after the schmitt trigger detects that a transient is present.

Each FIFO has an almost full/almost empty (AF/AE) flag that indicates when the number of words stored in the FIFO exceeds the programmable AF/AE offset value. The AF/AE flags are used in subsequent TD states to control the read and write strobes to each FIFO. The AF/AE offsets are programmed the first time the TD is reset, by taking $\overline{DAF}$ low and placing the desired value on the D0-D8 data inputs. The voltage FIFO uses an AF/AE offset of 32. This is programmed by connecting D5 to 5V and grounding the analog input to the

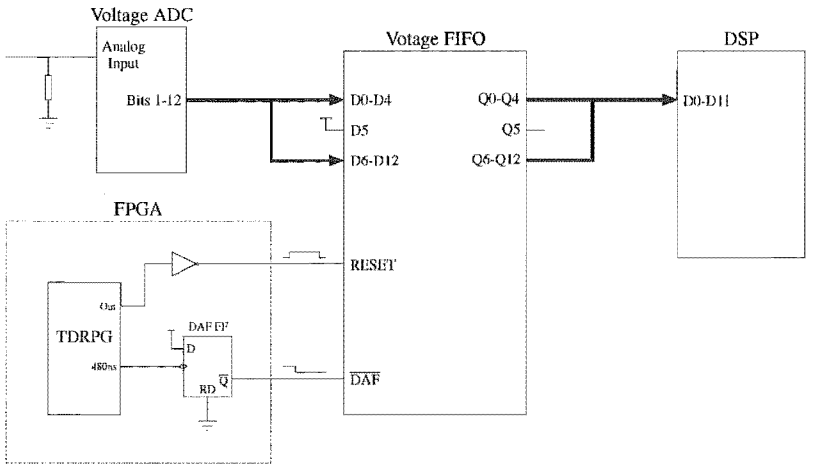

Figure 4.15 Voltage channel AF/AE offset hardware

ADC as illustrated in Figure 4.15. An ADC pulldown resistor ensures that D0-D4 and D6-D8 are 0 (they are connected to the 8 MSBs of the ADC) when no input signal is applied to the DAPM. Keeping $\overline{DAF}$ low ensures that the values are retained during subsequent reset cycles. A current FIFO offset of 64 is programmed by connecting D6 to 5V.

After power up the DSP runs software diagnostic tests to check that the AF/AE offsets values were programmed correctly. This is done by counting the number of write strobes received by each FIFO between the end of the reset cycle and AF/AE going low. The AF/AE software diagnostic test is discussed in 6.3.3.

4.8.2.2 Write State 1

Write state 1 is needed so that a 32 sample pre-transient window can be setup on each channel. Retaining the 32 most recent samples ensures that both analog signals are recorded prior to the voltage transient exceeding the schmitt trigger (see Figure 4.10) threshold. This enables a higher schmitt trigger threshold to be used (without fear of missing information) so that noise peaks do not activate the TD. The 100ns sampling period leads to a pre-trigger time of

$$Time_{pre-trigger} = 32 \cdot 100ns = 3.2\mu s \qquad (4.14)$$

At the completion of write state 1, the voltage FIFO AF/AE flag goes low, indicating that both FIFOs contain 32 samples. At this point the AF/AE flip-flop is reset (see Figure 4.13), causing ADC read strobes to pass to the each FIFO, and the TD to enter the next state. An LED is turned on indicating that the TD is ready to capture data. During manual testing sequences (operator activates IGM), the LED signal indicates to the operator that the system is ready for a test.

4.8.2.3 Read-Write State

The read-write state is needed to maintain a pre-transient window size of 32 samples. This is achieved by simultaneously reading and writing to each FIFO, so that the 32 most recent samples are kept.

To read a word from a FIFO, it's output enable must be high when a read strobe is applied. This causes the FIFO to drive the DAPM system bus. To avoid bus contention during the read-write state, words must be read from the voltage and current FIFOs at different times during the 100ns ADC convert cycle. This is accomplished by using the convert strobe (CONV) to read the voltage FIFO and $\overline{\text{CONV}}$ to read the current FIFO with non-overlapping pulses driving the respective output enable pins. The timing of these events is illustrated in Figure 4.16. FPGA propagation delays ensure that the 1ns hold time requirement is meet.

The DSP must also be removed from the system bus during the read-write state to avoid bus contention. This is accomplished in the DAPM application software by taking the DSP idle as soon as the TD is reset. The DSP is re-activated by the current AF/AE interrupt generated during write state 2, as explained in the next section. After power-up, FPGA control logic enables the TD to be reset 4 times before the DSP must go idle. These four resets are used for initialisation, the ENOBs test, and the voltage and current AF/AE tests. After the 5th reset, the system is ready for transadmittance function testing.

4.8.2.4 Write State 2

During write state 2, FIFO read strobes are gated off and both FIFOs begin to fill. When the current FIFO contains 64 samples it's AF/AE flag changes state, causing a DSP interrupt to be generated, taking the DSP out of the idle state. This leads to the following sequence of

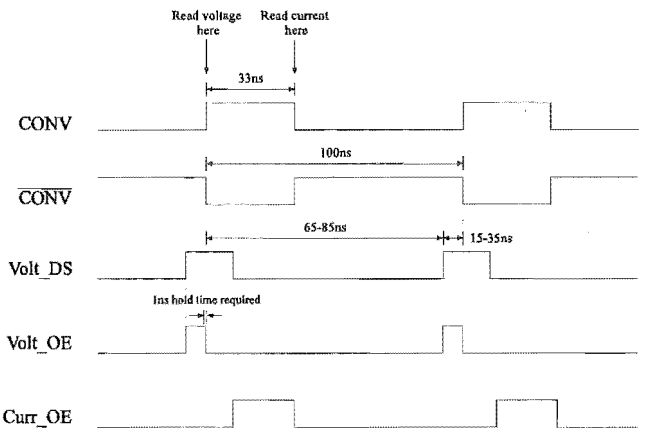

Figure 4.16 FIFO output enable strobe timing relationship

events:

- **DMA controller activated:** The current AF/AE ISR activates the DMA controller which transfers current FIFO samples to internal RAM. Internal RAM is used as the DMA bus cycle is reduced by one clock cycle, resulting in more data being transferred before the FIFO fills.
- **Current FIFO fills:** Because the DMA data transfer rate (5.55Mword/s) is less than the ADC sampling rate (10Mword/s), the current FIFO soon fills. When the current FIFO fills it's full flag changes state, causing a DSP interrupt to be generated. The current full ISR stops the DMA controller. The TD then enters the read state.

Writing to and reading from the current FIFO simultaneously increase the effective buffer size. The dual transfer process is illustrated in Figure 4.17, showing an effective filling rate of 4.45Mwords/s. Because DMA transfers start when the FIFO contains 64 words it takes

$$\frac{(1024-64)\text{ words}}{4.45\text{ Mwords/s}} = 216\mu s \tag{4.15}$$

for the FIFO to fill. The DMA controller can fill the 1k internal RAM block in

$$\frac{1024\text{ words}}{5.55\text{ Mwords/s}} = 185\mu s \tag{4.16}$$

This allows 1024 words to be transferred before the current FIFO fills, resulting in an effective buffer size of 2k. A current channel time window of 204.8μs is long enough to capture the transformer current response.

4.8.2.5 Read State

The read state is needed so that the DSP can transfer digitized data to external data RAM for processing. The following sequence of events occur when the TD enters the read state.

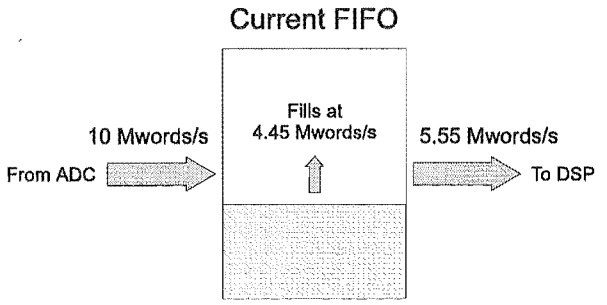

Figure 4.17 Current FIFO read and write data transfer rates

- **Empty current FIFO:** After the current FIFO fills its contents are transferred to external data RAM. This results in the transfer of another 1024 words, that are appended to those transferred by the DMA controller during write state 2.
- **Empty voltage FIFO:** At the completion of the above transfer, the voltage FIFO is full, and it's 1024 samples are transferred to external data RAM. The DSP is not interrupted by the voltage FIFO full event (interrupt enable bit disabled). The DSP instead checks the corresponding interrupt flag in the IF register to make sure that the event has occurred. A 1024 sample buffer is sufficient for the voltage channel as the supplied excitation has a time duration much less than 102.4μs (time window length of voltage channel).

During the read state the DSP primary bus drives the output enable pins of each FIFO, causing them to place the word being read onto the system bus. FPGA control logic is used to switch the FIFO output enable driving source as the TD cycles through it's different states during the data acquisition process. FPGA schematics are attached in Appendix J.

At the completion of the above transfers, the DAPM application software issues an interrupt acknowledge bus cycle, causing the TD to enter the reset state, allowing the cycle to repeat.

4.9 Digital Signal Processor

The most important consideration made when selecting the processor to be used for the TICMS design was the amount of development support available for it. Processing power was also an important consideration as the TICMS was designed to determine the TF in real time.

A DSP was used rather than a general purpose microprocessor as a DSP has on-chip hardware support for fast and efficient numerical processing operations and an instruction set that allows digital signal processing operations to be implemented with ease. Many DSPs also have on-chip hardware that allow multiple instructions to execute simultaneously.

A TMS320C31 DSP from Texas Instruments was chosen for the processor in the TICMS design for the following reasons:

- Development tools are available in the EEE Department including a C compiler, software simulator, debugger and in-circuit emulator.
- Extensive knowledge is available in the EEE Department as the C31 has been used in

other power system instrumentation projects.

- The C31 runs at 33MHz and is capable of 33.3MFLOPS allowing the required calculations to be performed in real time.
- The C31 is a floating point device which simplifies the software as code does not have to be written that accounts for integer overflow.
- The C31 is a cost-effective item which has benefits for a future commercial version of the system.

4.9.1 Description of the TMS320C31

The TMS320C31 is a high performance 32-bit floating point DSP that is capable of 33.3MFLOPS. The TMS320C31 can perform parallel multiply and ALU operations on both integer and floating point data in a single cycle. It has a general purpose register file, program cache, dedicated auxiliary register arithmetic units (ARAU), internal dual-access memories, a DMA channel for concurrent I/O, and a short machine-cycle time of 60ns. The TMS320C31 also has a 16Mword linear address space, internally and externally generated wait-states, two timers, a serial port, a multiple interrupt structure and a flexible boot program loader. A block diagram of the TMS320C31 is shown in Figure 4.18. The following sections describe features of the TMS320C31 that were utilised during the TICMS design.

4.9.1.1 Registers

The TMS320C31 has two sets of registers, the CPU registers and the memory-mapped peripheral registers. The CPU registers consist of

- **Extended-precision registers (R0-R7):** These are general purpose registers that are capable of storing and supporting operations on 32-bit integer and 40-bit floating-point data.
- **Auxiliary registers (ARU0-ARU7):** These are primarily used by the CPU and the ARAUs for the generation of addresses. They can also be used as general purpose registers.
- **Status register (ST):** This contains global information relating to the state of the CPU. It is also used to control the operation of the cache.
- **Interrupt enable register (IE):** This is used to enable and disable CPU and DMA interrupts.
- **Interrupt flag register (IF):** This indicates pending interrupts.

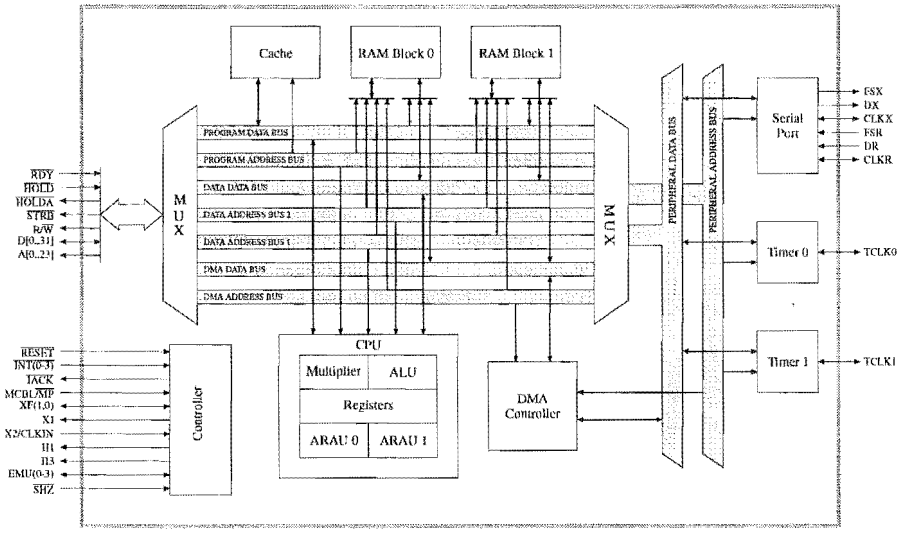

Figure 4.18 TMS320C31 DSP

- **I/O flags register (IOF):** This controls the function of the I/O pins, XF0 and XF1.
- **Data-page pointer (DP), Index registers (IR0, IR1), Block-size register (BK):** These are used for various addressing modes
- **Stack pointer (SP):** This contains the address of the top of the stack.
- **Program counter (PC):** This contains the address of the next instruction to be fetched.
- **Repeat-count register (RC), Block-repeat registers (RS, RE):** These are used for repeating a block of code.

The memory-mapped peripheral registers are used to control the operation of the primary bus, the serial port, the DMA controller and the two timers.

4.9.1.2 Memory Organisation

The TMS320C31 has a 16Mword linear address space that contains program, data and I/O space. The memory map is dependant on whether the processor is run in microprocessor mode ($MC / \overline{MP} = 0$) or microcomputer/boot loader mode ($MC / \overline{MP} = 1$). For the TICMS the TMS320C31 is run in microcomputer/bootloader mode and the memory map is as illustrated in Figure 4.19.

Included in the memory map are two internal RAM blocks, the memory-mapped peripheral registers, the interrupt and trap vectors, locations used by the boot program loader, and the user space. The TICMS use of the user space is also shown in Figure 4.19 and includes the mapping of the following devices

- External static RAM

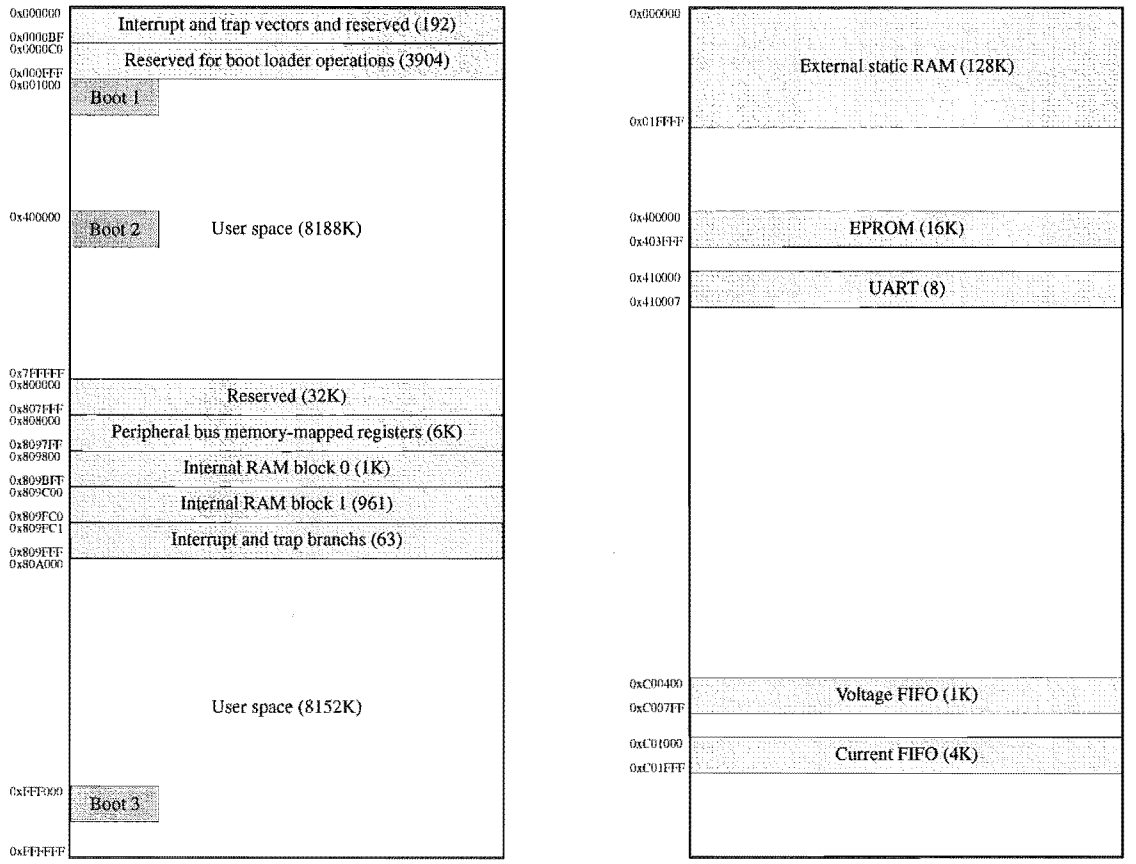

Figure 4.19 TMS320C31 memory map and TICMS use of the memory map

- EPROM
- UART
- Voltage channel FIFO
- Current channel FIFO

4.9.1.3 External Bus Operation

The TMS320C31 external bus consists of a 32-bit data bus, a 24-bit address bus and a set of control signals. The bus can be used for data, program and I/O accesses and has an external $\overline{\text{RDY}}$ signal for wait state generation. The bus also supports software-controlled wait states, bank switching and a hold operation. These functions are controlled through the memory mapped primary bus control register.

All bus cycles comprise of an integral number of H1 clock cycles where H1 is an internal clock derived from an external 33MHz crystal oscillator module. One H1 clock cycle is defined to be from one falling edge of H1 to the next and is 60ns in duration. For full speed (zero wait-state) accesses, writes take two H1 cycles and reads take one H1 cycle. However if the read follows a write takes then it takes two H1 cycles. Full speed read and write cycle

timing is illustrated in Figure 4.20. When either cycle is in progress $\overline{STRB}$ is low for the active portion of that cycle. The TICMS uses $\overline{STRB}$, R/$\overline{W}$ and the output of address decoding logic to generate the chip selects and strobes required to access each device.

The important parameters in Figure 4.20 are

- **Read access time:** This represents the amount of time that a device has to get its data on the data bus when the TMS320C31 is performing a read.
- **Data setup time:** This represents the amount of time that the TMS320C31 has data on

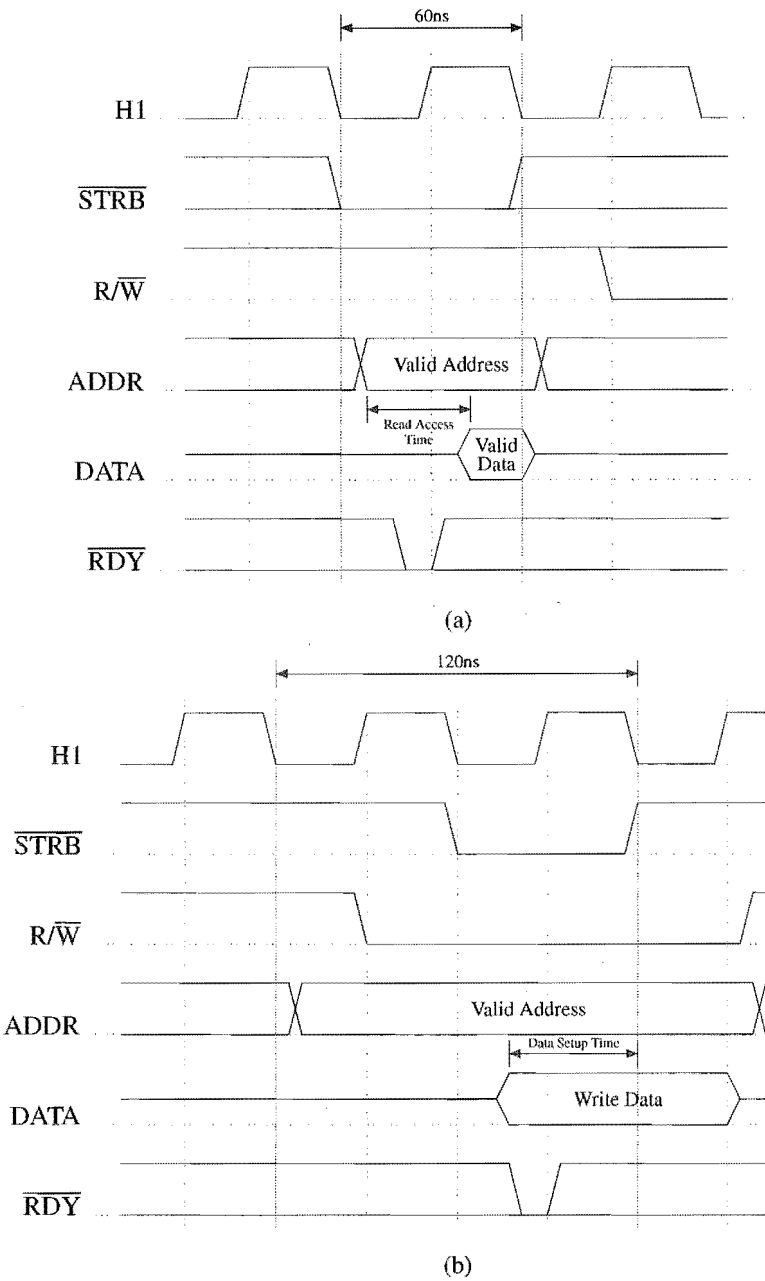

Figure 4.20 Bus cycle timing for (a) a processor read (b) a processor write

the data bus for before a write strobe is issued to a device when performing a write.

Under worst case timing conditions a zero wait-state read bus cycle requires the device to have a read access time of 30ns or better while a zero wait-state write bus cycle requires the device to operate with a data setup time of 40ns or less.

The TMS320C31 bus cycles can be extended to accommodate slower devices by inserting an integral number of wait-states. Wait-states can be inserted through hardware by delaying the activation of the $\overline{RDY}$ signal in Figure 4.20. This allows wait-states to be inserted only for those addresses to which the device is mapped. Alternatively wait-states can be inserted through software by writing to the primary bus control register. A given number of wait-states is then inserted for all addresses until the primary bus control register is next modified to change the number of wait-states. For the TICMS design all wait-states are inserted through software.

To determine the number of wait-states required for each device attached to the data bus it is necessary to compare timing parameters required by a device with those provided by the processor. Table 4-2 shows the number of wait-states required for each device.

Device	Wait-states for a read	Wait-states for a write
Static RAM	0	0
Voltage FIFO	1	1
Current FIFO	1	1
EPROM	4	4
UART	4	4

Table 4-2 Wait-states required for each device

4.9.1.4 Timers

The TMS320C31 has two general purpose 32-bit timer modules. The timers can be used to signal the processor or the external world at specified intervals, or can count external events. Each timer can interrupt both the CPU and the DMA controller. Associated with each timer is an I/O pin that can be used as an input clock, an output clock or a general purpose I/O pin. The following three memory mapped registers are used to control the operation of the timer:

- **Global-control register:** This is determines the operating mode of the timer, monitors

the timer status and controls the function of the timer's I/O pin.

- **Period register:** This specifies the timer's signaling frequency.
- **Counter register:** This contains the current value of the each timer.

For the TICMS design, timer0 is configured as a general purpose I/O pin and has a red LED attached. This LED is used to signal a test failure to the user when the system is running diagnostic tests. Further details can be found in Chapter 6. Timer1 is used to implement a delay function in software and is also used when the system runs the TD AF/AE diagnostic test. This test operates by using the timer to count the number of write strobes that each FIFO receives from the time that the TD is reset until the time the AF/AE flag is activated. When the processor detects that the AF/AE flag has changed state it stops the timer. The AF/AE offset is then stored in the counter register. Each FIFO is tested in turn through the use of a JK flip-flop that toggles the select input of a multiplexer each time the TD is reset. This is illustrated Figure 4.21. The select flip-flop is put into a known state after a hardware reset so that the same FIFO is tested first each time. Further TD AF/AE diagnostic test details can be found is 6.3.3.

4.9.1.5 DMA

The TMS320C31 has an on chip DMA controller that can perform input/output operations without interfering with the CPU. A DMA transfer consists of a read from a memory location and a write to a memory location. The DMA controller can read from and write to any location in the TMS320C31 memory map. The operation of the DMA is controlled with the following four memory mapped registers:

- **DMA global-control register:** This determines the state in which the DMA controller operates and indicates its status. It is updated with every cycle.
- **DMA source address register, DMA destination address register:** 24-bit registers

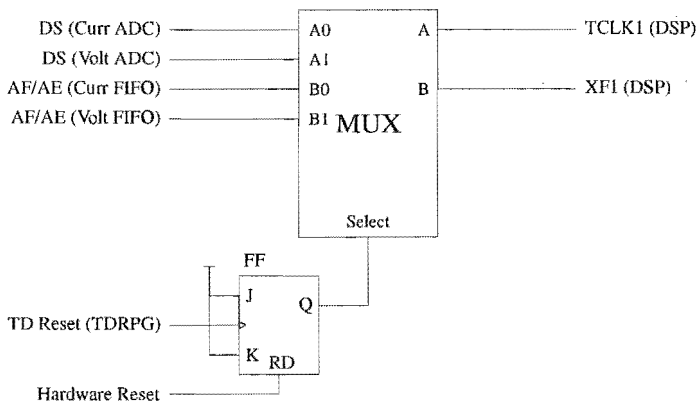

Figure 4.21 Support hardware for the AF/AE diagnostic test

that is used specify the DMA transfer source and destination addresses. The DMA controller can be configured to automatically update the addresses at the end of a transfer.

- **DMA transfer counter register:** A 24-bit register that is used to control the size of the DMA transfer.

The TICMS uses the DMA controller to transfer data from the current FIFO of the TD to internal RAM. The transfer happens while the TD receives new data from the analog-to-digital converters, thus increasing the effective buffer size as was explained previously.

4.9.1.6 Interrupt Structure

The TMS320C31 supports four external interrupts and five internal interrupts that can interrupt either the CPU or the DMA controller. Interrupts that occur simultaneously are serviced in the priority order indicated in Table 4-3. The interrupt vector table (IVT) located at the beginning of the address space includes a vector for each interrupt. Each vector contains the address of the interrupt service routine (ISR) for the interrupt. The vectors are specified in the source code and the IVT is loaded as a separate section when the system starts.

Interrupt	Priority (0=highest)	TICMS Use
$\overline{\text{RESET}}$	0	Hardware reset
$\overline{\text{INT0}}$ - external 0	1	Current FIFO AF/AE
$\overline{\text{INT1}}$ - external 1	2	Current FIFO full, boot loader mode
$\overline{\text{INT2}}$ - external 2	3	Voltage FIFO full, TD reset
$\overline{\text{INT3}}$ - external 3	4	UART
XINT0 - serial transmit	5	*Not used*
RINT0 - serial receive	6	*Not used*
TINT0 - timer 0	7	*Not used*
TINT1 - timer 1	8	AF/AE diagnostic tests, delay function
DINT - DMA controller	9	TD current channel data transfer

Table 4-3 TMS320C31 interrupts and their use

An external interrupt is detected when one of the $\overline{\text{INTn}}$ input pins is driven low. The

corresponding bit in the IF register is then set. If the corresponding bit in the IE register is set then the current thread of execution is suspended and the processor branches to address of the ISR as specified in the IVT. Internal interrupts operate in the same manner. All interrupts can be initiated and cleared prior to service by writing to the IF register.

An interrupt acknowledgement signal can be generated by activating the $\overline{\text{IACK}}$ output pin through software. $\overline{\text{IACK}}$ is not used for this purpose in the TICMS design, instead it is used as an output pin for resetting the TD as discussed in 4.8.2.1.

For a single interrupt to be recognized, external interrupts must be held low for between one and three H1 clock cycles. Figure 4.22 shows the hardware used to generate external interrupt pulses in the TICMS design. In this circuit external interrupts are held low for two H1 cycles and are synchronized with respect to H1.

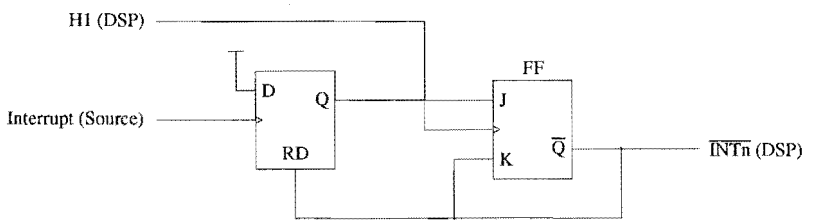

Figure 4.22 Interrupt pulse generator

4.9.1.7 Data Formats

The TMS320C31 supports two integer data formats and three floating-point data formats. The integer formats are 16-bit two's-complement integer format and a 32-bit two's-complement single-precision format. The floating point formats are a 16-bit short floating-point format, a 32-bit single-precision floating-point format and a 40-bit extended-precision floating-point format.

Data arriving from the analog-to-digital converters is in 12-bit two's-complement format and is converted to 32-bit two's-complement single-precision format and then to 32-bit single-precision floating-point format through software so that digital signal processing operations can be performed. After processing is completed a software module is used to convert all resultant data into IEEE single-precision floating-point format so that it can be interpreted on the attached PC.

4.9.1.8 Boot Loader Operation

Placing the TMS320C31 in microcomputer/boot loader mode allows the processor's on chip boot loader to load and execute programs that are received from a host processor, an

EPROM or other memory device. The programs to be loaded can reside in one of three memory mapped areas identified as Boot 1, Boot 2 and Boot 3 in Figure 4.19. Alternatively they can be received by means of the serial port. The boot loader mode is determined by activating one of the external interrupt pins after the processor comes out of reset. Table 4-4 shows the boot loader mode selected by each interrupt pin. After the interrupt pulse, the processor begins reading from boot location specified by the active interrupt.

For the TICMS design the processor boots from EPROM mapped to the Boot 2 location as shown in Figure 4.19. This EPROM is referred to as boot memory. The boot memory contains multiple blocks of code and data that are transferred to separate destination addresses at startup. A header that defines the organisation of the boot memory must be appended to the start of the first block. It must specify the boot memory width, the number of wait states required to access it, the block size and the destination address of the block. For the TICMS design four consecutive reads are required to transfer a 32-bit word from the 8-bit wide EPROM. To load another block at a different destination address, a new block size and destination address are appended to the end of the previous block. This is repeated for all blocks to be loaded. The boot loader completes the loading process when it encounters 0x00000000 appended to the end of a block in boot memory. The processor then begins executing from the destination address of the first block loaded.

Active Interrupt	Boot Loader Mode
$\overline{\text{INT0}}$	External memory load from Boot 1 (0x001000)
$\overline{\text{INT1}}$	External memory load from Boot 2 (0x400000)
$\overline{\text{INT2}}$	External memory load from Boot 3 (0xFFF000)
$\overline{\text{INT3}}$	Serial port load

Table 4-4 Boot loader selection

For the TICMS design, all blocks in EPROM are transferred to fast external static RAM. System performance is improved when running application code from static RAM as it can be accessed with zero wait-states.

4.10 Memory Interface

The following three memory interfaces are included in the TICMS design

- **SRAM:** Used for program and data memory.

- **EPROM:** Used for nonvolatile code storage.
- **FIFOs:** Used for rate buffers in the TD design.

4.10.1 SRAM

Four 128Kx8 SRAM chips are connected in parallel to produce 128Kx32 of SRAM. Figure 4.23 shows the SRAM interface to the DSP. Access is controlled by two signals, $\overline{CE}$ and R/$\overline{W}$. $\overline{CE}$ is activated by address decoding logic when the DSP addresses the SRAM locations. A read is performed when $\overline{CE}$ is low and R/$\overline{W}$ is high while a write is performed with $\overline{CE}$ and R/$\overline{W}$ low. When $\overline{CE}$ is high the SRAM data pins are placed in HiZ which allows other bus cycles to take place.

For a full-speed zero wait-state SRAM interface the DSP requires a read access time of 30ns or less. However the address decoding logic used introduces a 10ns delay under worst case timing conditions so that the required read access time is degraded to 20ns. As 20ns SRAM chips are used in the TICMS design then the zero wait-state requirements are only just satisfied. The TICMS software inserts one wait-state into SRAM bus cycles to ensure that they don't fail due to the marginal timing. This has little affect on system performance.

The SRAM is used for program and data memory. For the TICMS design, 8K of SRAM is reserved for program storage. As the current version of the application software uses 5K then future software modifications can be accommodated. The application software uses 10K for data storage, allowing the remaining 110K of memory to be used to buffer data prior to being sent to the PC. This allows the system to store the results of up to 110 previous tests depending upon how much data per test is stored.

4.10.2 EPROM

A 512Kbit EPROM arranged as 64Kx8 is used for non-volatile storage of DSP application software. The EPROM interface is shown in Figure 4.24. Access is controlled through two signals, $\overline{E}$ and $\overline{G}$. $\overline{E}$ is activated by address decoding logic when the EPROM is addressed

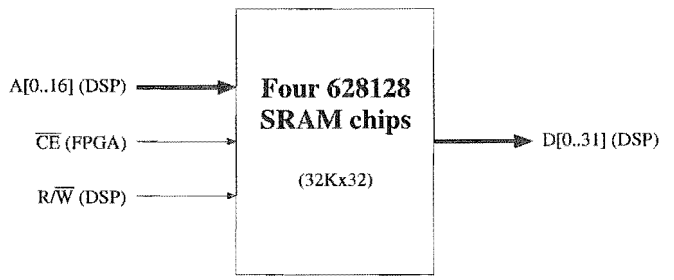

Figure 4.23 SRAM interface

and is used to select the device. $\overline{G}$ is driven by inverted $R/\overline{W}$ from the DSP and is used to enable the data outputs during a read.

At startup the DSP's on-chip boot loader transfers the contents of EPROM to SRAM which allows the application code to be run from the much faster SRAM. Four consecutive reads are performed to transfer each 32-bit word. Little-endian byte ordering is used when the EPROM is programmed to maintain compatibility with the boot loader.

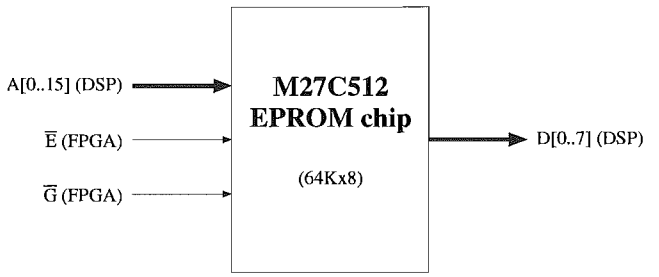

Figure 4.24 EPROM interface

4.10.3 FIFO

As previously discussed a FIFO is used in each of the DAPM channels to buffer the DSP from incoming data.

4.11 UART Interface

A 16550AF UART was used to interface the DAPM to an attached PC so that insulation test results could be graphed for easy interpretation. A UART was used for the following reasons:

- Availability of third party software for asynchronous serial I/O.
- Allows up to 10m of separation between the DAPM and the PC.
- Difficult to interface DSP's serial port directly to the PC.
- Provides a flexible communication interface.
- Allows some of the same UART routines to be used in both the DSP and Win95 application software.
- Allows the DSP application software to be downloaded from a PC using a monitor program stored in EPROM.

The DAPM is designed as Data Terminal Equipment (DTE). Since the IBM PC to which

the DAPM is attached also appears as a DTE then a null modem is required to connect the two. For the TICMS design a null modem cable is used to cross the input and outputs.

4.11.1 Description of the UART

The 16550AF is a 16-byte FIFO UART. FIFOs in both the receiver and transmitter sections reduce the number of interrupts presented to the DSP, thus reducing software overhead. The 16550AF adds or deletes standard asynchronous communication bits (start, stop and parity) that are used to form the serial data unit (SDU). The device has a programmable baud rate generator that divides a reference clock by 1 to $(2^{16}-1)$ to generate a master clock that is 16 times the baud rate. The 16550AF also features an independent receiver clock that allows the transmitter and receiver to operate at different baud rates. Other features include false start bit detection, internal diagnostics capabilities and a fully prioritized interrupt system.

As shown in Figure 4.25, the DAPM UART design consists of three interfaces: the system bus, the clock and the RS-232 I/O. Each of these interfaces along with the internal registers and the interrupts of the UART are discussed in the sections to follow.

4.11.1.1 System Bus Interface

The system bus is used to read and write the internal registers of the UART. Bytes to be transmitted, bytes received, control bytes and status information are passed between the DSP and the UART over the system bus.

To transmit a byte using the system bus the DAPM application software places the outbound byte into the transmitter FIFO. The UART then shifts the byte into the transmitter shift register when the latter is empty from where it is transmitted serially. To receive a byte the DAPM application software reads the receiver FIFO. The UART transfers all bytes

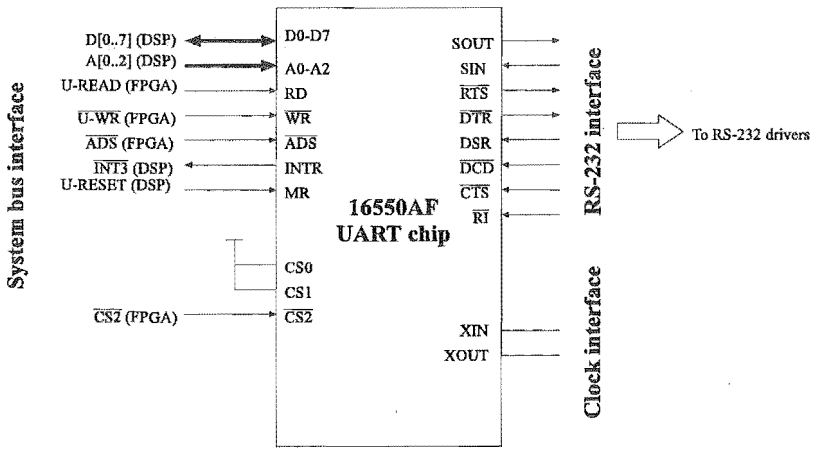

Figure 4.25 DAPM UART Interface

received from the receiver shift register to the receiver FIFO.

The system bus interface includes an interrupt signal that can inform the DSP when one of several internal conditions occur. The UART interrupts are discussed in 4.11.1.5.

4.11.1.2 Clock Interface

For the DAPM design the UART's reference clock is internally generated by connecting a 1.8432MHz crystal via the clock interface in Figure 4.25. The reference clock is divided by the divisor in the internal baud rate divisor latch to produce the master data clock. For the 16550AF the master data clock is 16 times the desired baud rate, thus fixing the clocking factor at 16. The baud rate divisor latch divisor is therefore determined as follows

$$\text{Divisor} = \frac{\text{Reference clock frequency}}{16 \times \text{desired baud rate}}$$

Because the master data clock is used to sample the serial input at 16 times the baud rate then the receiving UART is able to synchronise close to the center of the START bit. This provides maximum immunity from errors produced by sampling creep when the transmitter and receiver baud rates are slightly different. A clocking factor of 16 allows the baud rates to differ by 5.6% for a fast receiver and 4.3% for a slow receiver [5].

The master data clock is internally connected to the transmitter logic only. This makes it possible for the receiver and transmitter to operate at different baud rates. For the TICMS design the master data clock is connected to the receiver logic externally so that both receiver and transmitter operate at the same baud rate.

The DAPM UART is programmed to operate at a baud rate of 57600 bps. The maximum baud rate of 115200 bps was not used as this exceeds the ratings of the RS-232 line drivers used and is too restrictive on the maximum allowable RS-232 cable length between the DAPM and the attached PC.

4.11.1.3 RS-232 Interface

As shown in Figure 4.25, the DAPM design only uses the following RS-232 interface signals:

- **SOUT:** Serial Output (output)
- **SIN:** Serial Input (input)
- $\overline{\textbf{RTS}}$ **:** Request to Send (output for DTE)

- $\overline{\text{CTS}}$: Clear to Send (input for DTE)

SOUT and SIN are used to transmit and receive serial data respectively while $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$ are used as a handshake pair to establish communication. Further details on the communication protocol can be found in 6.4.2.

RS-232 line drivers are used to change the TTL level RS-232 signals from the UART to ±10V as required by the RS-232 standard. An AD232 line driver was selected for the DAPM design. The AD232 includes two on-chip charge pump voltage converters which convert the +5V input from the DAPM power supply to the ±10V needed to generate the RS-232 output levels.

4.11.1.4 Internal Registers and FIFOs

The 16550AF has nine internal registers and two FIFOs that can be accessed through software. Only ten locations need to be uniquely addressed as the transmitter and receiver FIFO are read write versions of the same address. A0-A2 alone only allow eight locations to be addressed. A control bit in the line control register allows an additional register to be accessed. For the DAPM design the two FIFOs and the internal registers are mapped to consecutive addresses as shown Figure 4.19. The name and function of the two FIFOs and each of the internal registers is as follows:

- **Receiver FIFO:** A 16-byte FIFO that holds received bytes.
- **Transmitter FIFO:** A 16-byte FIFO that holds bytes awaiting transmission.
- **Interrupt enable register:** Used to enable/disable individual UART interrupts.
- **Interrupt identification register:** Identifies the source of the highest priority pending interrupt.
- **Line control register:** Used to specify the SDU to be used.
- **MODEM control register:** Used to control the state of the RS-232 outputs and the general purpose outputs.
- **Line status register:** Used to report errors and status information.
- **MODEM status register:** Used to report a change in the state of the RS-232 inputs.
- **Scratch pad register:** Can be used as a byte of RAM.
- **Baud rate divisor latch:** Used to set the baud rate.

4.11.1.5 Interrupts

The UART's sole response to an interrupt is to assert the DSP's external interrupt, $\overline{\text{INT3}}$.

The UART itself is not responsible for supplying the address of the associated interrupt handler. The UART interrupt handler therefore reads the interrupt identification register whose contents are converted to the address of the correct subfunction to handle the pending interrupt. The UART supports the following interrupts:

- **Serialization error or BREAK:** Signals either an error or that S_{out} is being held low.
- **FIFO receiver trigger level:** Signals that FIFO receiver holds at least its programmed trigger level number of bytes.
- **FIFO timeout:** Signals that receiver FIFO has been holding a number of bytes below the trigger level more than a certain amount of time.
- **Transmission buffer empty:** Signals that the UART is able to receive another byte for transmission.
- **RS-232 input:** Signals that one of the RS-232 inputs: $\overline{DCD}$, $\overline{RI}$, DSR or $\overline{CTS}$ has changed state.

For the DAPM design the serialization error, FIFO timeout, and transmitter buffer empty interrupts are serviced by the DAPM application software.

4.12 FPGA Design

Included in the DAPM design is miscellaneous logic that is used to perform address decoding, chip select generation, interrupt generation, control and any other logic required to connect the different parts of the system together. Collectively this logic is referred to as glue logic. For the DAPM design all glue logic was implemented using a Xilinx FPGA. The use of an FPGA offers the following advantages over discrete logic chips:

- A single FPGA can replace hundreds of discrete logic chips so that much smaller PCB design sizes result.
- As a result of the above, system costs are reduced.
- Discrete logic chips often dissipate much more power.
- An FPGA can be completely reconfigured at the end of the design process without modifying the PCB layout. Hardware bugs are therefore easily fixed and are not nearly as costly as in a discrete logic chip design.
- Detailed timing simulations can be performed that take into account propagation delays throughout the FPGA. This allows performance critical designs to be easily verified. Simulating a discrete logic chip design to this level requires the use of very powerful and expensive software that takes PCB interconnect delays into consideration.

- The use of an FPGA substantially reduces system development time thus reducing a products time to market.

4.12.1 Xilinx FPGAs

A Xilinx FPGA consists of a matrix of configurable logic blocks (CLBs), a perimeter of I/O blocks (IOBs) and interconnect resources. The general structure of a device is shown below in Figure 4.26. Each CLB has a combinational logic section, two flip-flops and an internal control section. Combinational logic functions are implemented using small lookup tables (16x1 RAMs) while static memory cells are used in the control section for storing configuration information. IOBs provides an interface between the external package pin of the device and the internal user logic.

The XC3130A-3 FPGA used for the DAPM design contains a 10x10 matrix of CLBs. The current version of the FPGA firmware utilises about 65% of the FPGA's resources. A variety of packages are available for the device. A 100-pin quad flat pack (QFP) with 80-pins available for I/O was used. At present only 65 of these are used. The remaining I/O pins were routed to unused system signals during the DAPM PCB designed. This allows the system configuration to be changed at a later date and provides maximum flexibility when dealing with hardware bugs.

The FPGA design was carried out using the XACT development software from Xilinx. This software provides a development environment which includes the following components:

- Schematic entry software (supplied by a third party vendor).
- Partitioning placing and routing (PPR) software that maps the user design from high

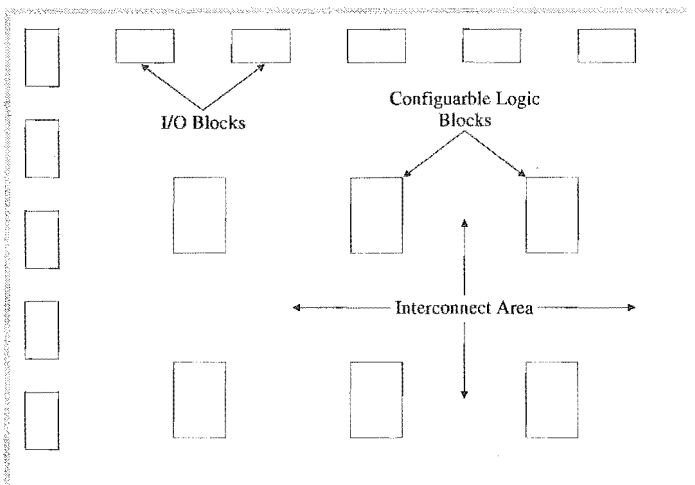

Figure 4.26 FPGA device structure

level schematics to the CLBs and IOBs of the FPGA.

- Simulation software that performs both logical and detailed timing simulations.
- Design editor software for modifying and inspecting the user's design at the chip level.
- Software that generates a serial PROM or EPROM hex file from the design configuration data.

The following four options are available for programming an FPGA using the configuration data resulting from a schematic design:

- **Master serial mode:** Allows FPGA configuration to be loaded from a serial PROM. In this mode the FPGA supplies the configuration clock for loading the data.
- **Master parallel mode:** Allows FPGA configuration to be loaded from a byte-wide EPROM.
- **Peripheral mode:** Allows FPGA configuration to be loaded from a host processor.
- **Slave serial mode:** Allows FPGA configuration to be loaded from a serial PROM. In this mode the serial PROM supplies the configuration clock for loading the data.

For the DAPM design the FPGA configuration can be loaded using both master serial and slave serial modes. A jumper on the PCB is used to select between the two. When the system was first being tested slave serial mode was used to download the configuration from a PC running the development software, via a serial cable connected to the serial PROM socket. Design changes could be made to the schematics and a new configuration created and downloaded in less than 10 minutes.

Once a stable configuration was obtained the development software was used to produce a serial PROM and the FPGA loaded using master serial mode. When in master serial mode the configuration process is initiated as soon as the power is turned on. For the DAPM design an LED attached to the FPGA that indicates when the configuration is complete. See the DAPM schematics given in Appendix J for the FPGA configuration interface.

4.12.2 TICMS FPGA Logic

FPGA logic modules are used to implement the following:

- **TD control logic:** Used to control the data acquisition process by taking each FIFO through different states according to the arrival of external events. The TD interface was discussed in 4.8.
- **Address decoding logic:** Used to generate chip select and enable signals for the

different DSP peripherals as they are addressed in software.

- **Interrupt pulse generation:** Used to generate interrupt pulse signals compatible with the DSP requirements upon the arrival of monitored external (to the DSP) events.
- **UART interface:** Used to interface the DSP and UART bus cycles together.
- **System reset circuitry:** Used to put the DAPM into a known state after power-up and upon a hardware reset.
- **Diagnostic test support logic:** Used to support the FIFO AF/AE diagnostic tests conducted by software during the start-up sequence.

4.13 Power Supply

A bench-top linear power supply provides the DAPM with DC power. A switching power supply was not used as they produce conducted noise, radiated noise and electric and magnetic fields that combine to degrade the SNR of the analog-to-digital converters. The dual ±8V linear supply feeds four voltage regulators that supply power to various parts of the board. The four regulators give rise to the following power supplies on the DAPM:

- **+5V Digital:** Supplies all digital components.
- **+5V Analog:** Supplies positive rail of all analog components, positive analog rail of ADCs and positive digital rail of ADCs via a pi filter.
- **-5.2V Analog:** Supplies negative rail of all analog components, negative analog rail of ADCs and negative digital rail of ADCs via a pi filter.
- **+5V Sampling:** Supplies sampling clock generator.

Care has been taken to isolate the digital and analog supplies as much as possible. This is necessary to prevent switching noise on the digital power supplies from coupling onto the analog supplies and degrading the performance of the ADCs. The sampling clock generator supply is isolated from the digital supplies in order prevent digital noise from causing timing jitter on the ADC's sampling clock. Because the sampling clock is itself a digital signal then it has the potential for causing noise in the analog portion of the system and is therefore isolated from the analog supplies.

Power planes within the PCB layer stack are used for each of the supplies above. Each supply is referenced to a separate ground plane and all ground planes are connected at a common star point that returns to the bench top power supply. Further layout details are presented in 4.14 while the PCB artwork is included in Appendix K. Heatsink thermal

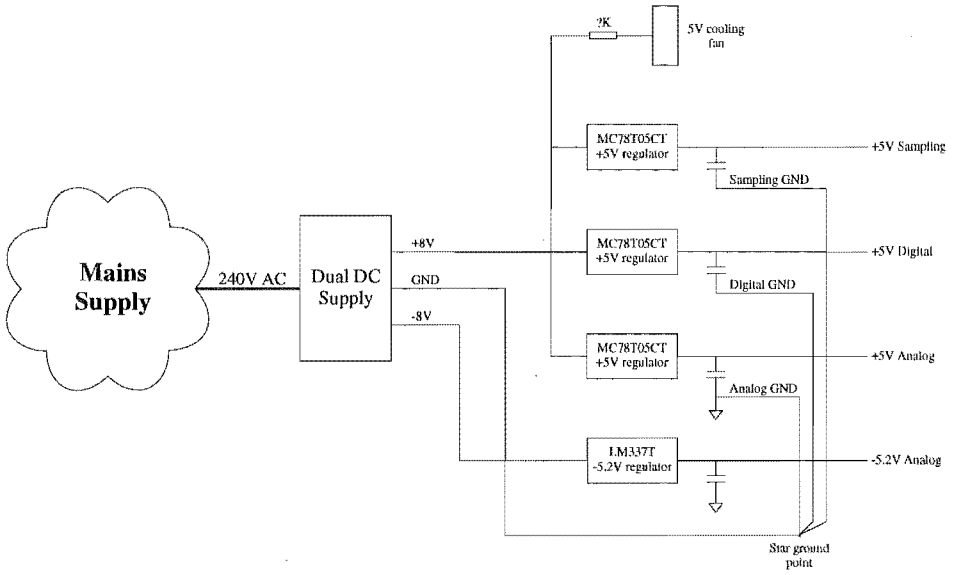

Figure 4.27 Power supply arrangement

calculations for each of the power supply regulators are presented in Appendix F.

The DAPM power supply arrangement is shown in Figure 4.27. The bench-top supply also powers a cooling fan as the DAPM has a worst-case power dissipation of 22.5W (see Appendix F). The IGM is powered separately and has its own built-in power supply.

Being separate instruments, the DAPM and the IGM are powered from separate ground referenced supplies. Both are powered from the same laboratory wall outlet socket, which forms a grounding star point for the TICMS. This grounding arrangement is shown in Figure 4.28, and shows that all grounds are connected to the common star point that is connected to the building ground.

The DAPM is not isolated because it sends data to an attached PC and is housed in a grounded metal enclosure. Because single ended signal transmission is used between the IGM and the DAPM, the IGM is powered from a ground referenced supply also. The IGM has both a ground referenced DC supply for the control circuitry, and an isolated DC supply that it used to generate the V_{dc} for the impulse generation circuitry in Figure 4.2.

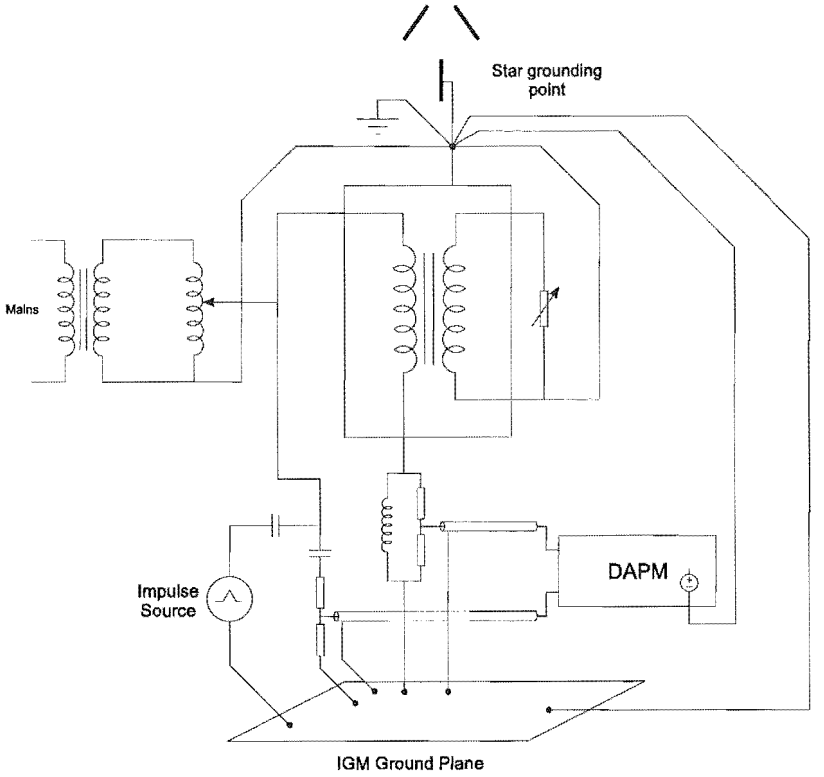

Figure 4.28 TICMS grounding arrangement

4.14 DAPM PCB Layout

An 220x100mm (standard Eurocard size) mixed signal 8 layer PCB was designed for the DAPM. The overall system layout is illustrated in Figure 4.29 while a photograph of the DAPM PCB is shown in Figure 4.29. The main layout objectives were

1. To isolate sensitive analog signals from noisy digital ones
2. To keep the signal paths as short as possible

During the layout different signals were isolated from each other to minimise system noise. High level analog signals were separated from low level analog signals, and analog signals were kept away from digital signals. Because the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal and is as liable to cause noise as any digital signal, it was kept isolated from both the analog and digital systems. Keeping signals paths as short as possible prevents the need for termination resistors due to transmission line effects in the digital section of the PCB, which is driven by a 33MHz clock signal.

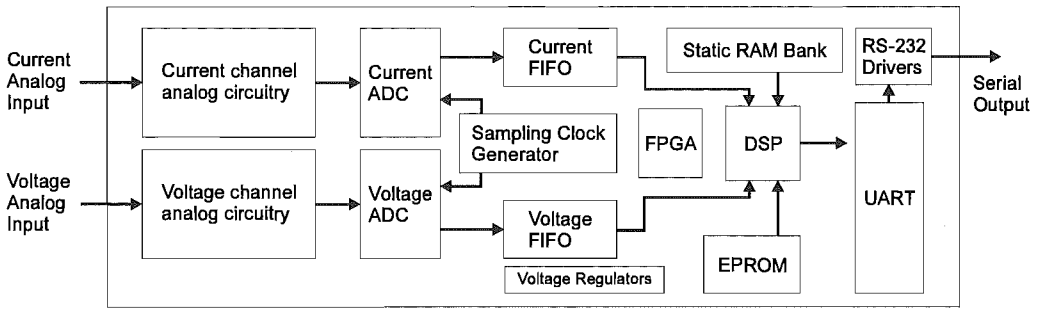

Figure 4.29 Overall DAPM PCB layout

The layer stack consists of 4 signal layers and 4 copper plane layers with the layer build in the following order:

- Top signal layer
- Analog and digital power plane layer
- Mid signal layer 1
- +5V power plane layer
- Mid signal layer 2
- -5.2V power plane layer
- Analog and digital power plane layer
- Bottom signal layer

Only 3 copper plane layers were required during the layout. Because an even number of layers must be used in the manufacture of a multi-layer PCB, the analog and digital ground plane layer was duplicated. For the layer build above, signal layers are separated by copper plane layers (creating a Faraday shield) which reduces coupling between them. The artwork for each layer is presented in Appendix K.

Other features of the DAPM PCB layout include:

- **Use of surface mount:** Surface mount components were used as much as possible as the use of surface mount in a high frequency system minimises parasitic capacitance and inductance associated with the device leads. Further the use of surface mount results in a more compact board layout which enables shorter high frequency signal paths.
- **Sockets were avoided:** The use of IC sockets can add resistance, inductance and capacitance to a circuit and may degrade performance to an unacceptable level. For this reason sockets were avoided. No sockets were used on the expensive DAPM ADCs. The only socketed components used were the EPROM (DIP socket so that it could be

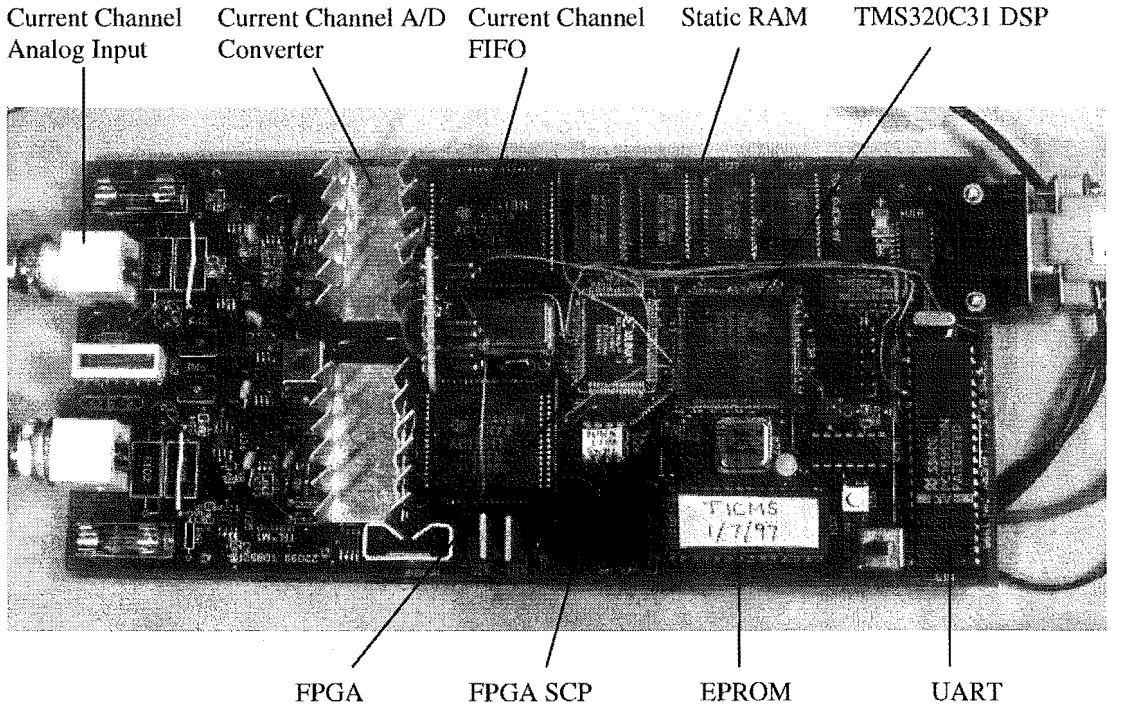

Figure 4.30 DAPM PCB

reprogrammed), SCP (DIP socket so that it could be reprogrammed), and FIFOs (socket for PLCC packaging)

- **Use of decoupling capacitors:** The power supply inputs were decoupled to the ground plane using good quality, low ESL, ESR tantalum electrolytic capacitors. This bypasses low frequency noise to the ground plane. Low inductance ceramic capacitors were at each power pin of each IC to provide high frequency decoupling. Surface mount chip capacitors were used for minimum inductance. Small tantalums were also used around IC power pins to provide low frequency decoupling.

- **Separate ground planes:** Separate analog and digital ground planes were used that were connected at a star grounding point, located at the common return for the power supplies. Sensitive analog components, including the ADCs, were decoupled to the analog ground plane.

- **Separate power supplies:** Separate power supplies were used for the analog and digital circuits. This was achieved by dividing the copper power plane layers into different sections as the artwork in Appendix K shows. The analog supply pins of ADCs were powered directly from the analog supply. Pi filters were used between the analog supply and the digital supply pins of the ADCs. All ADC power supply pins were decoupled to the analog ground plane.

- **Through hole vias used:** All vias used were through hole making all conductor nodes accessible from either side of the PCB. The use of blind and buried vias results in internal conductor nodes and connections within the layer stack that are not accessible

to the outside world. This can render a manufactured PCB useless if there are any layout errors.

- **Shielding:** The DAPM was housed in a grounded metal enclosure that acts as a Faraday shield. A PCB mounting metallic shielding plate was used over the analog section of the DAPM. This was used to minimise the effects of any radiated noise from the digital section. These shielding precautions are necessary as the DAPM has been designed to operate in the harsh electromagnetic environment next to an energised power transformer in the field.

4.15 Conclusions

The developed TICMS prototype system has been tested in the University of Canterbury EEE Department's Power Instrumentation Laboratory to ensure that it is functionally behaving as designed. Results from test procedures performed in the laboratory are presented in the Chapter 7. The next stage is to install the system in a field situation and monitor its performance to ensure compliance with requirements and to evaluate its usefulness.

4.16 References

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Chapter 5

SIGNAL PROCESSING

The purpose of this chapter is to describe the signal processing principles used in the design of the TICMS and the application of those principles to the problem of determining the transadmittance function to 3MHz with sufficient accuracy. In the first section a general overview of the signal processing system along with its requirements is presented. The second section describes the sampling and quantisation operations that take place during data acquisition and discusses the influence of these operations on the TICMS design. Next the design of the transducers employed in the TICMS and their intentional affect on the signals being acquired is described. The following sections present some underlying Fourier theory needed to understand subsequent TICMS signal processing operations. These include the computationally efficient FFT algorithm used in the TICMS design and the signal processing operations needed to determine the transadmittance function magnitude and phase from the acquired signals. The final two sections discuss the application of signal averaging and zooming techniques that are optionally applied in order improve the accuracy of the calculated transadmittance function.

5.1 Overview

The prime objective of the signal processing operations used is to ensure that the transadmittance function is determined with sufficient accuracy and up to the required frequency in 'real-time' As a result, for a potential system to be successful, it must satisfy the following two requirements:

- The signal processing operations must be performed with an accuracy that will ensure the calculated transadmittance function does not vary from one insulation test to the other when no winding faults are present. Failing to achieve this results in faults being incorrectly diagnosed or missed, making the system useless.
- The computational requirements of the signal processing operations must be such that they can be performed in 'real-time' with existing DSP/μP hardware. The definition of

real-time used here is such that the required computations can be completed, and a fault detected within 100ms, before the fault can cause transformer failure. If this requirement is not meet then transformer failure may take place before preventative action can be initiated, reducing the usefulness of the system.

To satisfy these requirements the following measures were taken during the TICMS design:

- Software signal processing operations have been implemented in MATLAB and trialed with real data. This enabled their accuracy and correctness to be evaluated and reduced development time as operations could be quickly trialed before being committed to DSP code.
- Software signal processing operations have been implemented using a 32-bit floating point DSP that is capable of 33.3MFLOPS.

An overview of the major signal processing related operations implemented in the TICMS is given in Figure 5.1, where a distinction is made between those implemented in hardware and those in software. Each of the processing stages shown, along with their features that contribute to the transadmittance function being determined to 3MHz in real-time, are described in the sections to follow.

5.2 Data Acquisition

The approach taken by the TICMS to determine the transadmittance function is one of

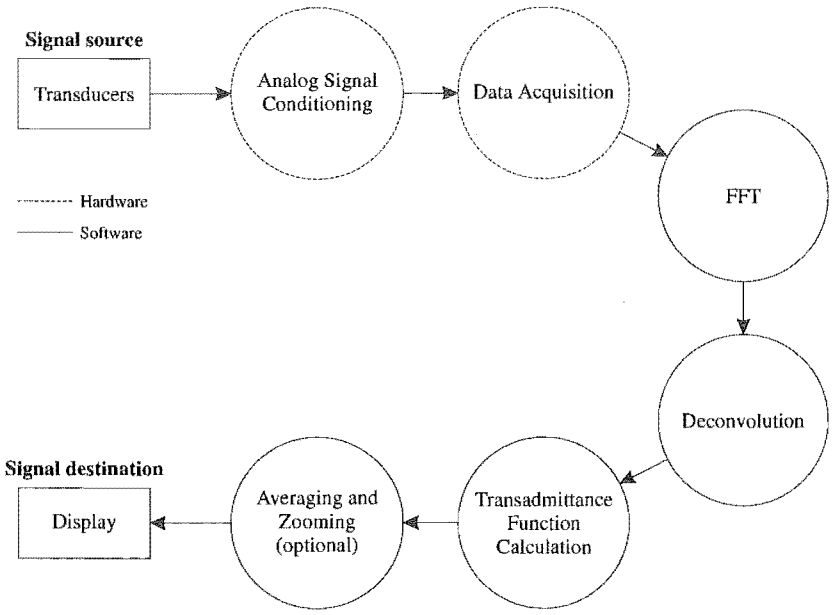

Figure 5.1 Major signal processing related operations implemented in the TICMS

digital signal processing in software as is indicated in Figure 5.1. Before these operations can be applied however, it is necessary to digitise the analog signals from the transducers. Digitisation is a two step process that involves first sampling an analog signal at discrete instants in time and then quantising the resulting sample amplitudes for use in a finite word length machine. This section discusses the sampling and quantisation operations as they relate to the TICMS design and also the TICMS design features that are a direct result of these operations.

5.2.1 Signal Sampling

The sampling process is accomplished by multiplying each signal by the following sampling function

$$\delta_{T_s}(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \tag{5.1}$$

where

$$T_s = \frac{1}{f_s} \tag{5.2}$$

and f_s is the sampling frequency. If the voltage or current channel signal is represented by x(t), then sampling results in

$$\hat{x}(t) = \sum_{n=-\infty}^{\infty} x(nT_s)\delta(t - nT_s) \tag{5.3}$$

which is a set of uniformly spaced samples, T_s seconds apart as illustrated in Figure 5.2(c). Because multiplication in the time domain corresponds to convolution in the frequency domain then the spectrum of the sampled signal, $\hat{X}(f)$, is obtained by convolving X(f) with $\Delta_{T_s}(f)$. This results in $\hat{X}(f)$ being equal to the X(f) repeated every f_sHz as shown in Figure 5.2(c).

For there to exist a one-to-one mapping between the continuous signal and it's samples the sampling frequency must be chosen to satisfy the requirements of the Nyquist sampling theorem. This states that the signal must be band-limited to f_a such that

$$f_s \geq 2f_a \tag{5.4}$$

If this condition is not met then the part of the spectrum centered at f_s in Figure 5.2(c) will overlap with that centered at the 0 making it impossible to fully recover X(f), a condition

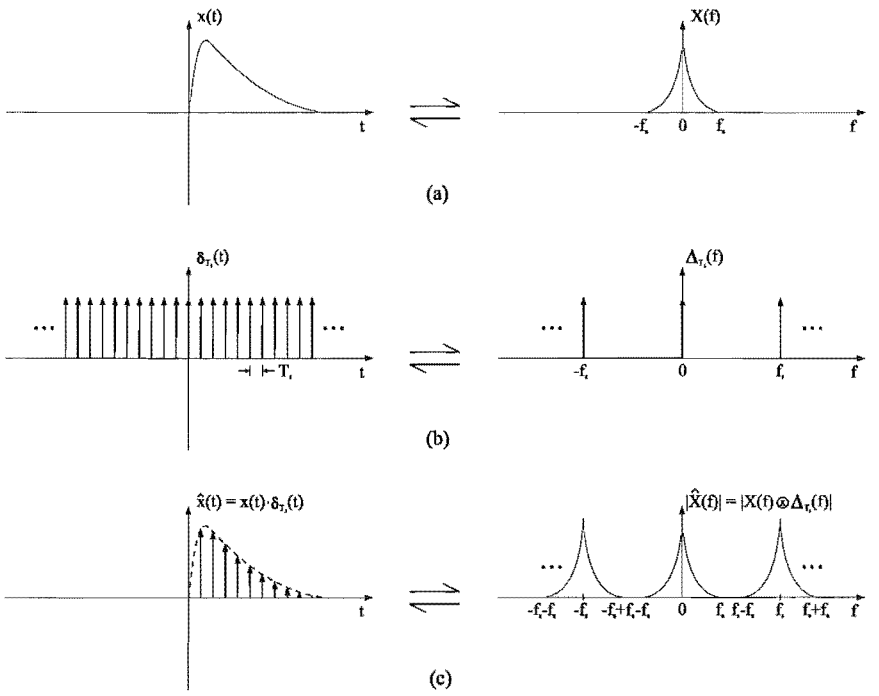

Figure 5.2 Sampling of a signal

known as aliasing.

5.2.2 Quantisation

Quantisation occurs when the continuous sample amplitudes are represented by a discrete set of amplitudes for use in a finite word length machine. This results in a quantisation error that has a maximum instantaneous value equal to half of a quantisation step. For an N-bit digitiser a quantisation step is equal to

$$\Delta = \frac{V_{fs}}{2^N} \tag{5.5}$$

where V_{fs} represents the full-scale analog input voltage, as is indicated in Figure 5.3 for a 3-bit quantiser with twos complement output coding. If there are a large number of small quantisation steps, the quantisation error signal resembles a series of straight lines that extend from -Δ/2 to Δ/2 with varying slopes. The exception occurs when the signal goes through a maximum or a minimum within a quantisation step. To calculate the rms quantisation error it is first necessary to consider the error over a single step as shown. This error, ε(t'), is represented as follows

$$\varepsilon(t') = st' \tag{5.6}$$

where

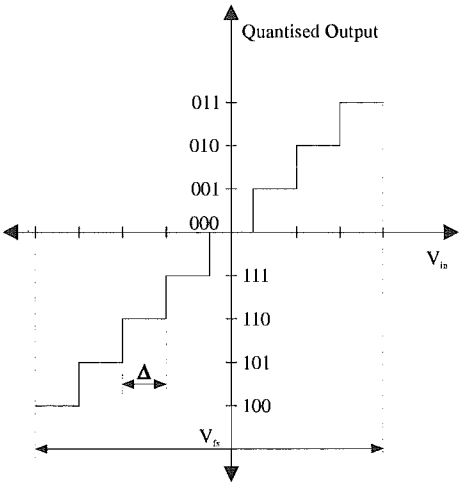

Figure 5.3 Input-output characteristic of a 3-bit quantiser

$$\frac{-\Delta}{2s} < t' < \frac{\Delta}{2s} \tag{5.7}$$

The rms value of $\varepsilon(t')$ is then calculated as follows

$$\varepsilon_{rms} = \sqrt{\frac{s}{\Delta}\int_{-\Delta/2s}^{\Delta/2s}(st')^2 dt'} = \frac{\Delta}{\sqrt{12}} \tag{5.8}$$

Because ε_{rms} is constant and independent of the slope of $\varepsilon(t')$, then the total rms quantisation error can be expressed as

$$QE_{rms} = \frac{\Delta}{\sqrt{12}} \tag{5.9}$$

when there are a large number of small quantisation steps. The rms SNR ratio for N-bit quantisation with a full-scale sinusoidal input is then calculated as follows

$$SNR = \frac{V_{rms}}{QE_{rms}} = \frac{V_{fs}/2\sqrt{2}}{\Delta/\sqrt{12}} = \frac{2^N\sqrt{3}}{\sqrt{2}} \tag{5.10}$$

where V_{rms} is the rms value of the input sinusoid. Expressing the SNR in dB results in

$$SNR = 20\log_{10}\left(\frac{2^N\sqrt{3}}{\sqrt{2}}\right) = 6.02N + 1.76 \text{ dB} \tag{5.11}$$

which is used to calculate the level of the quantisation noise floor for an N-bit digitiser. The TICMS uses 12-bit ADCs which gives a SNR of 74dB. This places the quantisation noise floor at -74dB where 0dB represents a full-scale ADC input.

5.2.3 Effective Number of Bits

The effective number of bits (ENOBs) criteria is used to evaluate the overall performance of the TICMS data acquisition system. The ENOBs must be determined as it is not equal to that for the ADCs as given in the manufacturers data sheet.

Considering the system in terms of the ENOBs takes into account all error sources including quantisation errors, ADC errors, sampling clock jitter, system noise and distortion introduced by analog signal conditioning circuitry. To calculate the ENOBs the signal to noise and distortion ratio (SINAD) is needed. Using the SNR in Eq. (5.11) results in an ENOBs better than that produced by the system as the SNR does not include sampling clock jitter, system noise and distortion errors introduced by the analog front end. The ENOBs is calculated from the SINAD by rearranging Eq. (5.11) as follows

$$\text{ENOBs} = \frac{\text{SINAD} - 1.76}{6.02} \tag{5.12}$$

Two methods are commonly used to measure the ENOBs, one based on time domain analysis and the other on frequency domain analysis. In applying the time domain procedure a full-scale sinusoid is digitised. The best fit sinewave is then found by minimising the mean squared error. This is then subtracted from the digitised sinusoid to reveal the noise and distortion. Varying the frequency of the input sinusoid allows the ENOBs to be determined as a function of frequency. The frequency domain procedure uses the FFT algorithm to transform the digitised sinusoid into the frequency domain. The SINAD is then determined by noting the level of the system noise floor below ADC full-scale.

The TICMS approximates the frequency domain procedure by instead digitising an impulse from the IGM. The measured SINAD is 55dB below full-scale. The results in an ENOBs of 9. The fact that the input impulse only occupies half of the bipolar input voltage range accounts for the loss of 1-bit. The 'apparent' loss of the other 2-bits can be attributed to the fact that the ADCs used have a 2V analog input voltage range, making a quantisation step equal to 488μV. Therefore just 2mV of analog noise is enough to account for the 2-bit loss.

A common misconception regarding ENOBs is that any resolution beyond the ENOBs is useless. This is not true. To see this, the rms value of the error sources included in the SINAD is broken into two parts as follows

$$\text{TE}_{\text{rms}} = \sqrt{\text{QE}_{\text{rms}}^2 + \text{OE}_{\text{rms}}^2} \tag{5.13}$$

where TE_{rms}, QE_{rms} and OE_{rms} represent the rms values of the total error, quantisation error and other errors respectively. If the bits below the ENOBs are dropped then QE_{rms} and

hence TE_{rms} increase. This decreases the SINAD and therefore the ENOBs.

5.2.4 Anti-Alias Filtering

Aliasing is often avoided in practice by low pass filtering a signal prior to sampling and then sampling at a rate such that aliasing is negligible. The level below which aliasing is negligible is the signal noise floor whose minimum value is equal to the level of the quantisation noise floor, as given by Eq. (5.11). This represents a base level below which aliased signals will not be resolved by the ADCs and allows a low pass anti-aliasing filter response to be derived as in Figure 5.4(a). The order of the filter must be selected so that at least AdB of attenuation takes place from f_c to $f_s/2$ which represent the filter cut-off and Nyquist frequencies respectively. The filter specifications can be relaxed a little if aliasing is permitted in the transition band as illustrated in Figure 5.4(b). This is acceptable provided signal frequency components beyond f_c are not used. In practice this is often forced as real signals usually have frequency components beyond the cut-off that are below full power and are therefore attenuated below the quantisation noise floor.

The ADCs used in the TICMS design sample each channel at 10MHz with 12-bits of vertical resolution. The requirements of a potential anti-aliasing filter based on the response in Figure 5.4(b) has been indicated. Here f_c has been set equal to 3MHz, the bandwidth over which the transadmittance function is to be determined. In practice it is often desirable to set f_c above the bandwidth of interest as considerable magnitude and phase distortion can

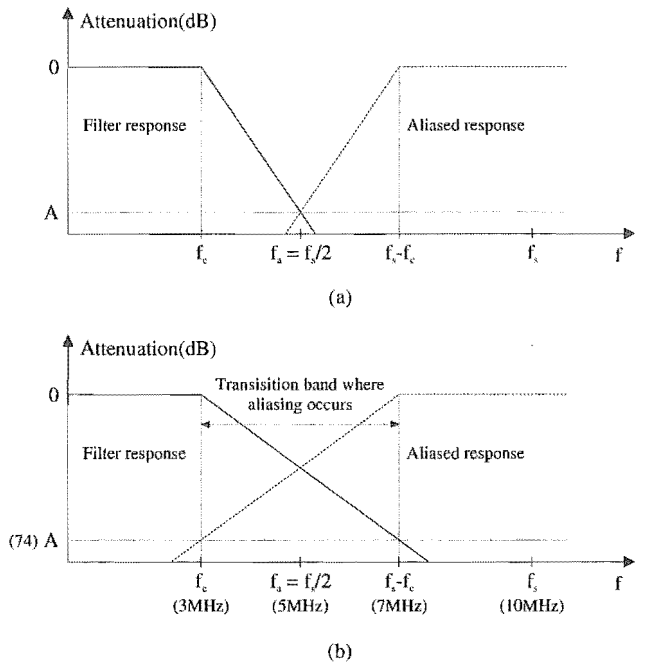

Figure 5.4 (a) Anti-aliasing filter response. (b) Less stringent response

occur in the vicinity of the cut-off frequency. For a maximally flat Butterworth response the required filter order is calculated from the specifications in Figure 5.4(b) as follows

$$n \geq \frac{\log_{10}(10^{0.1\alpha_s} - 1)}{2\log_{10}\omega_s} = 10.05 \qquad (5.14)$$

where ω_s is the stopband edge normalised to a cut-off of 1Hz. As far as the TICMS design is concerned the disadvantages of using an 11th order analog anti-aliasing filter are:

- It can be very sensitive to component variations which could introduce transadmittance function changes that may be incorrectly interpreted as being due to a winding fault.
- It requires much electronic componentry and can be difficult to design.
- It introduces considerable phase distortion making it very difficult if not impossible to calculate the transadmittance function phase.
- It's phase distortion prevents the use of the high pass filtering scheme used to increase the effective dynamic range of the digitisers.

The required filter order can be reduced by increasing the sampling rate and/or increasing the quantisation noise floor level. For the TICMS situation these changes occur simultaneously as increasing the sampling rate of the ADCs requires sacrificing vertical resolution. This approach was rejected for the following reasons:

- Sacrificing vertical resolution increases the noise floor and reduces the frequency to which the transadmittance function can be determined without making other system changes.
- Increasing the sampling rate requires faster and larger FIFO rate buffers between the DSP and the ADCs to cope with the increased data input rate. This would lead to a considerable increase in the chip count as 4 FIFO chips per channel would probably be required.
- Additional multirate digital signal processing would be required to implement a FIR anti-aliasing filter so that the data could be decimated before being processed by the FFT algorithm.
- For the current design the DAPM PCB operates at 30MHz. Further increases would make the PCB design much more difficult as well as making it more difficult to shield the analog circuitry from the high frequency noise generated by the ADC sampling clock.
- ADC's that sample above 30MHz with 10 or 12-bits of vertical resolution can be very expensive and often don't perform as well as is implied on the manufacturer's data sheet.

5.2.5 TICMS Excitation Characteristics

If the frequency content of the signal is known in advance then anti-alias filtering does not always need to be implemented. This is the case if all signal frequency components that are above the Nyquist frequency are below the signal's noise floor. To accomplish this and avoid the high order analog filter problems above, the TICMS design uses an impulse excitation with spectral characteristics tailored to meet this objective. The frequency at which the impulse's spectrum drops below the noise floor is controlled by adjusting it's rise and fall times as shown in Figure 5.5. The TICMS design uses a 0.5/5.8μs impulse waveshape that drops below the noise floor at around 2MHz. This frequency can be increased so that the transadmittance function can be determined to 3MHz, by further adjusting the impulse waveshape. However this has undesirable effects on the following parameters of the impulse generator circuit implementation:

- **Efficiency:** If too low then peak voltage of impulse will be small.
- **Output impedance:** If too high then the transducers and the transformer may cause significant loading.
- **Required electronic switch ratings:** If too demanding then the design may not be practical.

Another disadvantage of further waveshape modification is that it increases the magnitude of the high frequency components in the current response to the point where transformer resonances may make them appear above the Nyquist frequency. If this occurs then aliasing errors are introduced into the system. The TICMS avoids this dilemma by using a transducer design that allows independent control of the frequency at which each channels signal spectrum drops below the noise floor, as discussed below.

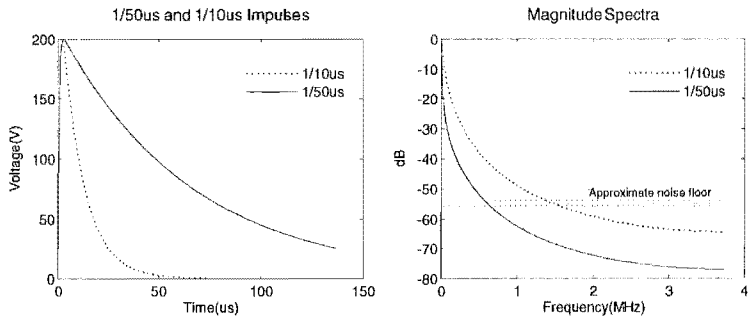

Figure 5.5 Affect of reducing impulse fall time on it's magnitude spectrum

5.3 Transducer Design

The TICMS uses a transducer design that attenuates the large magnitude low frequency

components in order to prevent them from taking up dynamic range as is illustrated in Figure 5.6. In addition, the analog attenuation on each channel is reduced so that the transducer outputs occupy the ADC full-scale. This method makes it possible to control the frequency at which the signal spectra drop below the noise by adjusting the following:

- The upper frequency of the low frequency band being attenuated.
- Each channels overall analog attenuation.

This approach allows the existing IGM design compromise to be maintained and is flexible as the transducer characteristics and channel attenuation can be easily changed to accommodate future requirements. Changing the characteristics of the generated impulse by too much requires redesigning the IGM.

To ensure that the transadmittance function can still be determined at the lower frequencies the TICMS uses the DAPM DSP to deconvolute the voltage and current channel transducer output signals, thereby reconstructing each signal to what it appears at the transformer. This is possible as each transducer is designed to ensure that the attenuated low frequencies are not attenuated below the signal's noise floor as indicted in Figure 5.6.

As discussed in 4.4.1, a first order high pass filter with a cutoff frequency of 1.53MHz is used for the voltage channel transducer, as shown in Figure 5.7. The effect of the high pass filter is illustrated in Figure 5.8 where V_{in} is the spectrum of the transducer output and V_{imp} is that of the transducer input obtained by deconvolution as explained in 5.6. Further, it is indicated in Figure 5.8 that if V_{imp} had been digitised directly, then it's spectrum would have dropped below the noise floor at 1.4MHz thus limiting the transadmittance function bandwidth. Therefore the use of the high pass filter allows the spectrum of V_{imp} to be determined to 4MHz and increases the effective dynamic range of the voltage channel digitiser by 40dB. The offset between V_{in} and V_{imp} is due to the R1 R2 resistive divider in Figure 5.7. The filter's frequency response including the effect of the divider is derived in

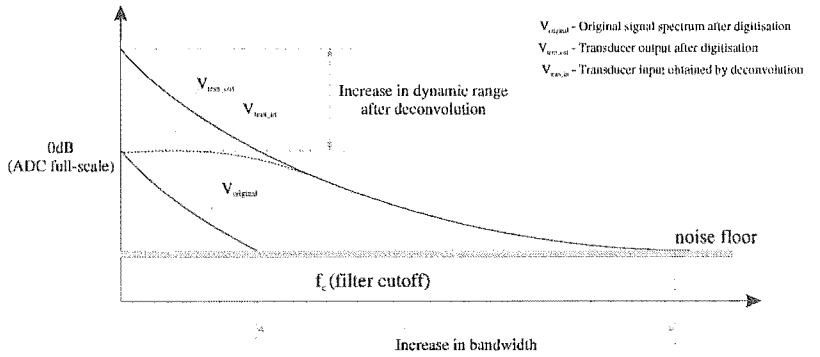

Figure 5.6 How the transducers affect the signal spectrum

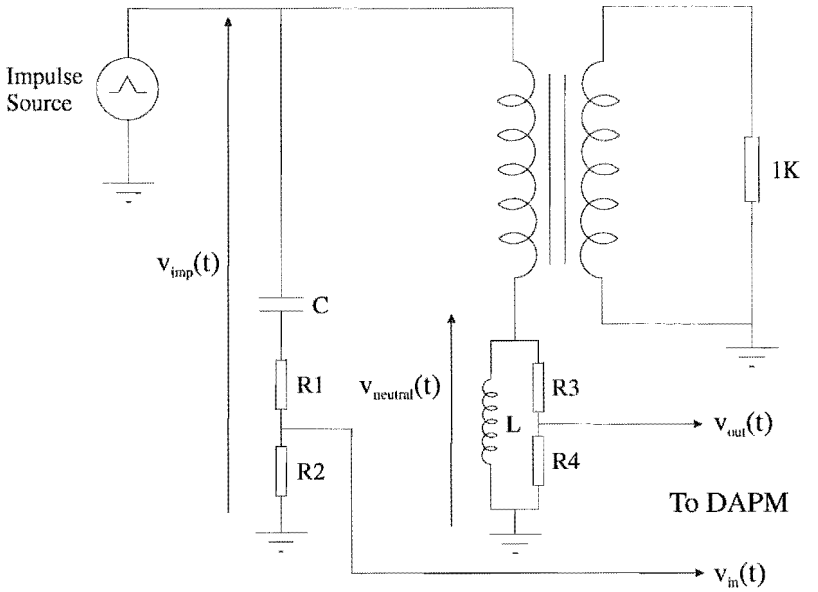

Figure 5.7 Voltage and current channel transducers

Appendix E.

An RL shunt is used to implement the current channel transducer as shown in Figure 5.7 and discussed further in 4.4.2. Because the reactance of the shunt increases with frequency, the voltage drop across it also increases with frequency when the magnitude of the current flowing through stays constant. This gives the RL shunt a high pass characteristic. The frequency response of the shunt is derived in Appendix E and the results are used to calculate the transadmittance function as described in 5.6. Further details on the shunt can be found in 4.4.2.

Further benefits of the transducer design that are related to signal digitising are:

- Adjustments are easily made that still allow the transadmittance function to be

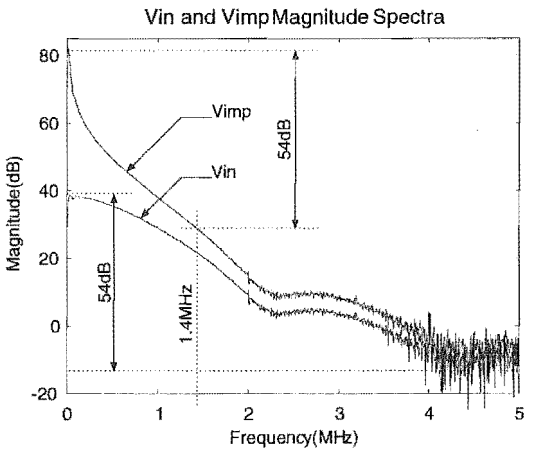

Figure 5.8 Voltage transducer signals

determined to 3MHz if the actual noise floor is higher than that expected at design time due to operating environment.

- Because independent control of the frequency at which the signal spectra drop below the noise floors is possible then the transadmittance function can be determined to 3MHz without introducing aliasing in the current channel.
- The use of the RL shunt prevents the need to window the current channel data as explained in 5.4.3.

5.4 Background Fourier Theory

Because a large proportion of the signal processing operations performed by the TICMS are based on Fourier theory, this section presents a brief description of the background information needed to understand later results.

5.4.1 Continuous Fourier Transform

Let x(t) denote a nonperiodic deterministic signal that is a function of time t. By definition, the Fourier transform of x(t) is given by the integral

$$X(f) = \int_{-\infty}^{\infty} x(t)e^{-j2\pi ft}dt \tag{5.15}$$

where the variable f denotes frequency. Given the Fourier transform X(f), the original signal x(t) is recovered exactly using the formula for the inverse Fourier transform

$$x(t) = \int_{-\infty}^{\infty} X(f)e^{j2\pi ft}df \tag{5.16}$$

The functions x(t) and X(f) are said to constitute a Fourier transform pair that is represented as follows

$$x(t) \Leftrightarrow X(f) \tag{5.17}$$

In general the Fourier transform X(f) is a complex function of frequency and can therefore be expressed in the form

$$X(f) = |X(f)|e^{j\Theta(f)} \tag{5.18}$$

where $|X(f)|$ and $\Theta(f)$ are called the continuous magnitude spectrum and continuous phase spectrum of x(t) respectively. Here the spectrum is referred to as continuous as the magnitude and phase of X(f) are defined for all frequencies.

Referring to Eq. (5.15) it is easily seen that for a real-valued time function x(t)

$$X(-f) = X^*(f) \tag{5.19}$$

where the asterisk denotes complex conjugation. It therefore follows from Eq. (5.19) that for a real-valued function

$$|X(-f)| = |X^*(f)| = |X(f)| \tag{5.20}$$

and

$$\Theta_{X(-f)}(f) = \Theta_{X^*(f)}(f) = -\Theta_{X(f)}(f) \tag{5.21}$$

Eqs. (5.20) and (5.21) allow the following statements to be made on the spectrum of a real-valued signal

- The magnitude spectrum of the signal is an even function of frequency, that is it is symmetric about the vertical axis.
- The phase spectrum of the signal is an odd function of frequency, that is it is antisymmetric about the vertical axis

These two statements are summed up by saying that the spectrum of a real-valued signal exhibits conjugate symmetry. The time domain signals processed by the TICMS are real-valued and therefore exhibit conjugate symmetry.

5.4.2 Discrete Fourier Transform

The discrete Fourier transform (DFT) provides an approximation to the continuous Fourier transform in which the both the time and frequency domain descriptions of a signal are represented in digital form, making it amenable to machine computation. The DFT can be derived by using the Trapezoidal rule to evaluate Eq. (5.15) numerically and is expressed as follows

$$X(k) = \frac{1}{N}\sum_{n=0}^{N-1} x(n)e^{-j2\pi nk/N} \quad k = 0, 1, \ldots, N-1 \tag{5.22}$$

where N is the number of time domain samples and x(n) and X(k) represent the discrete time and frequency domain descriptions respectively.

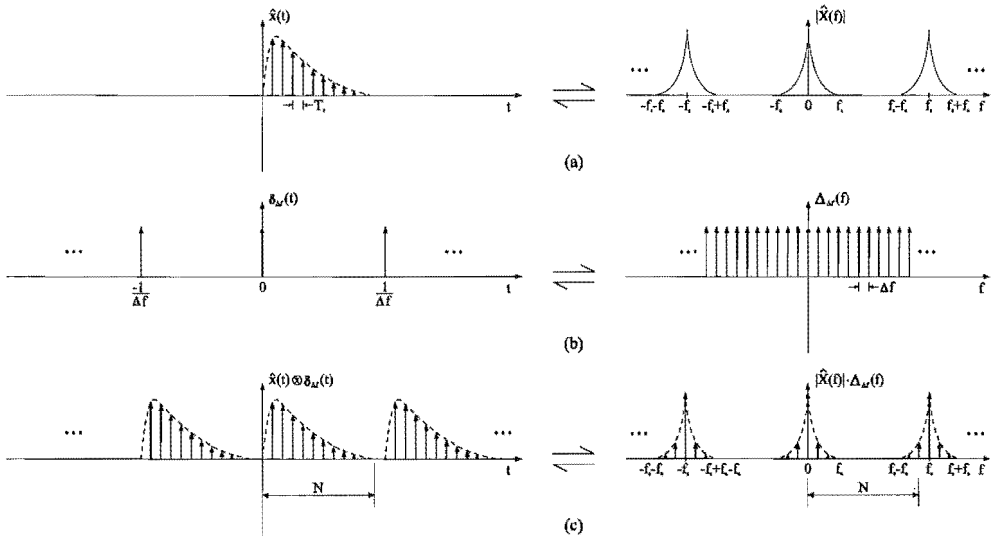

Figure 5.9 Discrete spectra results in time domain periodicity

Before the DFT can be applied it is necessary to truncate the time domain sequence to a finite number of samples as implied in Eq. (5.22). Furthermore for the resulting spectra in Eq. (5.22) to be discrete, it is necessary that the finite time domain sequence repeat periodically as illustrated in Figure 5.9(c). As a result of this assumed periodicity for the DFT, the spacing between frequency domain samples, the frequency deviation Δf, can be derived from Figure 5.9 as follows

$$\Delta f = \frac{1}{T_{period}} = \frac{1}{NT_s} = \frac{f_s}{N} \tag{5.23}$$

where T_{period}, T_s and f_s are the period of the repetition in the time domain, the spacing between time domain samples and the sampling rate respectively.

Referring to Figure 5.9(c), it is seen that the N frequency domain samples returned by the DFT are arranged as illustrated in Figure 5.10(a). It is therefore necessary to rearrange the results as in Figure 5.10(b) so that a more meaningful spectrum results when plotted. However, because the time domain signals transformed by the TICMS are real-valued then

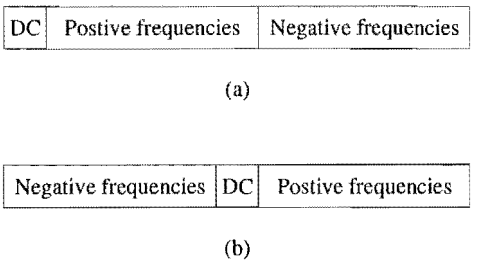

Figure 5.10 (a) Spectral components as returned by DFT. (b) After rearrangement.

the resulting spectra exhibit conjugate symmetry as explained in 5.4.1. For this reason only the positive frequencies are sent by the DAPM to the attached PC for display as discussed in 6.4.2

5.4.3 Windowing

As just mentioned it necessary to truncate the time domain sequence to a finite number of samples when using the DFT. Spectral leakage is said to have taken place when truncation results in one of the following conditions:

- For a transient signal nonzero samples are discarded.
- For a periodic signal the assumed periodicity of the DFT results in a periodic waveform that is different from that being transformed.

When spectral leakage takes place the spectrum of the signal differs from what would have been obtained if truncation had not caused either of the conditions above. In practice the errors introduced by spectral leakage are reduced by multiplying the time domain sequence by an appropriate window function that allows the sequence to gradually approach zero, as opposed to being abruptly truncated.

When transients are digitised windowing is not necessary if they naturally decay to zero before the end of the time record. For the TICMS the time record is determined from the sampling rate and number of samples taken as follows

$$\text{Time Record} = N \cdot T_s = 2048 \cdot 100\text{ns} = 204.8\mu\text{s} \tag{5.24}$$

As far as the TICMS is concerned, a transient is considered to have decayed to zero when it drops below the level of an ADC LSB and remains below this level so that it can no longer be resolved. Both of the transducer output signals digitised by the DAPM satisfy this requirement so that windowing does not need to be applied. Testing the transformers in Chapter 7 without the use of the RL shunt results in a current response that does not decay to zero within the data acquisition interval. Therefore without the use of the RL shunt, windowing would have been required to minimise spectral leakage errors as the DAPM rate buffer sizes and data transfer rates do not allow the time record to be increased. Finally future test setups may result in longer time signals being produced and therefore may require that the data be windowed.

5.5 The Fast Fourier Transform

The fast Fourier transform (FFT) is simply an algorithm that can calculate the DFT much

more rapidly than other available algorithms and is used by the TICMS to transfer the captured time domain data into the frequency domain.

To appreciate the need for the FFT algorithm it is first necessary to consider again the DFT

$$X(k) = \frac{1}{N}\sum_{n=0}^{N-1} x(n)W^{nk} \quad k = 0, 1, \ldots, N-1 \tag{5.25}$$

where

$$W = e^{-j2\pi/N} \tag{5.26}$$

Considering Eq. (5.25) for the case N = 8 results in 8 equations that can be represented in matrix form as follows

$$\begin{bmatrix} X(0) \\ X(1) \\ X(2) \\ X(3) \\ X(4) \\ X(5) \\ X(6) \\ X(7) \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & W^1 & W^2 & W^3 & W^4 & W^5 & W^6 & W^7 \\ 1 & W^2 & W^4 & W^6 & W^0 & W^2 & W^4 & W^6 \\ 1 & W^3 & W^6 & W^1 & W^4 & W^7 & W^2 & W^5 \\ 1 & W^4 & W^0 & W^4 & W^0 & W^4 & W^0 & W^4 \\ 1 & W^5 & W^2 & W^7 & W^4 & W^1 & W^6 & W^3 \\ 1 & W^6 & W^4 & W^2 & W^0 & W^6 & W^4 & W^2 \\ 1 & W^7 & W^6 & W^5 & W^4 & W^3 & W^2 & W^1 \end{bmatrix} \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ x(3) \\ x(4) \\ x(5) \\ x(6) \\ x(7) \end{bmatrix} \tag{5.27}$$

where

$$W^{nk} = e^{-j2\pi(qN+r)/N} = e^{-j2\pi r/N} = W^{(nk) \bmod N} \tag{5.28}$$

has been used to simplify. Using bold type to denote matrix quantities allows Eq. (5.27) to be written more compactly as follows

$$\mathbf{X(k)} = \mathbf{W}^{nk}\mathbf{x(n)} \tag{5.29}$$

Examination of Eq. (5.27) reveals that since $\mathbf{W}$ and possibly $\mathbf{x(n)}$ are complex then N^2 complex multiplications and N(N-1) complex additions are needed to perform the DFT calculation. For the TICMS design 2048 samples are taken on both the voltage and current channels and computation of the frequency spectra using Eq. (5.25) results in an excessive number of operations. To ensure that the TICMS is still able to determine the transadmittance function in real-time an FFT algorithm that dramatically reduces the number of complex multiplications and additions is used.

5.5.1 Decimation in Time FFT Algorithm

To develop the FFT implementation used in the TICMS design it is necessary to first consider again the DFT

$$X(k) = \frac{1}{N}\sum_{n=0}^{N-1} x(n)W^{nk} \quad k = 0, 1, \ldots, N-1 \tag{5.30}$$

and let the number of time domain samples taken satisfy

$$N = 2^{\gamma} \tag{5.31}$$

where γ is an integer. Because n and k take on all integral values between 0 and N-1 inclusive then Eq. (5.31) allows both to be represented in binary form as

$$n = n_{\gamma-1}2^{\gamma-1} + n_{\gamma-2}2^{\gamma-2} + \cdots + n_1 2^1 + n_0 2^0 \tag{5.32}$$

and

$$k = k_{\gamma-1}2^{\gamma-1} + k_{\gamma-2}2^{\gamma-2} + \cdots + k_1 2^1 + k_0 2^0 \tag{5.33}$$

where n_i and k_i can be 0 or 1. Eqs. (5.32) and (5.33) allows Eq. (5.30) to be rewritten as follows

$$X(k_{\gamma-1}, k_{\gamma-2}, \ldots, k_1, k_0) = \frac{1}{N}\sum_{n_0=0}^{1}\sum_{n_1=0}^{1}\cdots\sum_{n_{\gamma-2}=0}^{1}\sum_{n_{\gamma-1}=0}^{1} x(n_{\gamma-1}, n_{\gamma-2}, \ldots, n_1, n_0)W^p \tag{5.34}$$

where

$$p = (n_{\gamma-1}2^{\gamma-1} + \cdots + n_0 2^0)(k_{\gamma-1}2^{\gamma-1} + \cdots + k_0 2^0) \tag{5.35}$$

The key to reducing the number of complex operations required is in simplifying W^p in Eq. (5.34). To begin this process we first write

$$W^p = W^{n_{\gamma-1}2^{\gamma-1}(k_{\gamma-1}2^{\gamma-1} + \cdots + k_0 2^0)} \cdots W^{n_0 2^0(k_{\gamma-1}2^{\gamma-1} + \cdots + k_0 2^0)} \tag{5.36}$$

The first term in Eq. (5.36) can be simplified by writing the first term of it's power as follows

$$n_{\gamma-1}2^{\gamma-1}k_{\gamma-1}2^{\gamma-1} = n_{\gamma-1}k_{\gamma-1}2^{\gamma+\gamma-2} = n_{\gamma-1}k_{\gamma-1}2^{\gamma}2^{\gamma-2} \tag{5.37}$$

Operating on the remaining terms of it's power in the same way results in

$$W^{n_{\gamma-1}2^{\gamma-1}(k_{\gamma-1}2^{\gamma-1}+\cdots+k_0 2^0)} = W^{2^\gamma(n_{\gamma-1}k_{\gamma-1}2^{\gamma-2})}W^{2^\gamma(n_{\gamma-1}k_{\gamma-2}2^{\gamma-3})}\cdots W^{2^\gamma(n_{\gamma-1}k_1 2^0)}W^{2^\gamma(n_{\gamma-1}k_0 2^{-1})} \quad (5.38)$$

which is simplified to

$$W^{n_{\gamma-1}2^{\gamma-1}(k_{\gamma-1}2^{\gamma-1}+\cdots+k_0 2^0)} = W^{n_{\gamma-1}2^{\gamma-1}k_0} \quad (5.39)$$

since

$$W^{2^\gamma} = W^N = \left[e^{-j2\pi/N}\right]^N = 1 \quad (5.40)$$

Performing the above simplification on the second term in Eq. (5.36) results in

$$W^{n_{\gamma-2}2^{\gamma-2}(k_{\gamma-1}2^{\gamma-1}+\cdots+k_0 2^0)} = W^{n_{\gamma-2}2^{\gamma-2}(2k_1+k_0)} \quad (5.41)$$

Progressing through each of the terms in Eq. (5.36) and substituting the resulting simplifications into Eq. (5.34) produces

$$X(k_{\gamma-1},\ldots,k_0) = \frac{1}{N}\sum_{n_0=0}^{1}\cdots\sum_{n_{\gamma-1}=0}^{1}x(n_{\gamma-1},\ldots,n_0)W^{n_{\gamma-1}2^{\gamma-1}k_0}\cdots W^{n_0 2^0(2^{\gamma-1}k_{\gamma-1}+\cdots+k_0)} \quad (5.42)$$

which represents the foundation of the FFT algorithm used in the TICMS design. Performing the first inner summation in Eq. (5.42) and labeling the intermediate result we obtain

$$x_1(k_0, n_{\gamma-2},\ldots,n_0) = \sum_{n_{\gamma-1}=0}^{1}x_0(n_{\gamma-1},\ldots,n_0)W^{n_{\gamma-1}2^{\gamma-1}k_0} \quad (5.43)$$

where all terms that don't include $n_{\gamma-1}$ have been moved to the left of the summation and x(n) has been renamed to $x_0(n)$. Continuing to perform each of the summations in Eq. (5.42) separately results in the following equation set

$$\begin{aligned}
x_1(k_0, n_{\gamma-2},\ldots,n_0) &= \sum_{n_{\gamma-1}=0}^{1}x_0(n_{\gamma-1},\ldots,n_0)W^{n_{\gamma-1}2^{\gamma-1}k_0}\\
x_2(k_0, k_1, n_{\gamma-3},\ldots,n_0) &= \sum_{n_{\gamma-2}=0}^{1}x_1(k_0, n_{\gamma-2},\ldots,n_0)W^{n_{\gamma-2}2^{\gamma-2}(2k_1+k_0)}\\
&\vdots\\
x_\gamma(k_0, k_1,\ldots,k_{\gamma-1}) &= \sum_{n_0=0}^{1}x_{\gamma-1}(k_0, k_1,\ldots,k_{\gamma-2}, n_0)W^{n_0 2^0(2^{\gamma-1}k_{\gamma-1}+\cdots+k_0)}\\
X(k_{\gamma-1}, k_{\gamma-2},\ldots,k_0) &= \frac{1}{N}x_\gamma(k_0, k_1,\ldots,k_{\gamma-1})
\end{aligned} \quad (5.44)$$

where X(k) represents the DFT of $x_0(n)$. The above set of recursive equations represent the Cooley-Turkey decimation in time FFT algorithm when N is a power of 2.

5.5.2 Signal Flow Graph

To facilitate the development of FFT software a signal flow graph is used to represent Eqs. (5.44). The signal flow graph for the case N = 8 is given in Figure 5.11 where each vertical column of nodes corresponding to the intermediate results in Eqs. (5.44) is referred to as a computational array. In general there will be γ computational arrays where

$$N = 2^{\gamma} \tag{5.45}$$

Each node is entered by two transmission paths from nodes in the previous computational array where each transmission path brings a quantity from a node in one array, multiplies it by W^p or 1 and inputs the result into a node in the next array. Results that enter a node from two transmission paths are combined additively.

To see the relationship between Eqs. (5.44) and Figure 5.11 it is useful to consider the first summation in Eqs. (5.44) for the case N = 8

$$x_1(k_0, n_1, n_0) = \sum_{n_2=0}^{1} x_0(n_2, n_1, n_0) W^{4n_2k_0} \tag{5.46}$$

Enumerating the equations represented by Eq. (5.46) results in

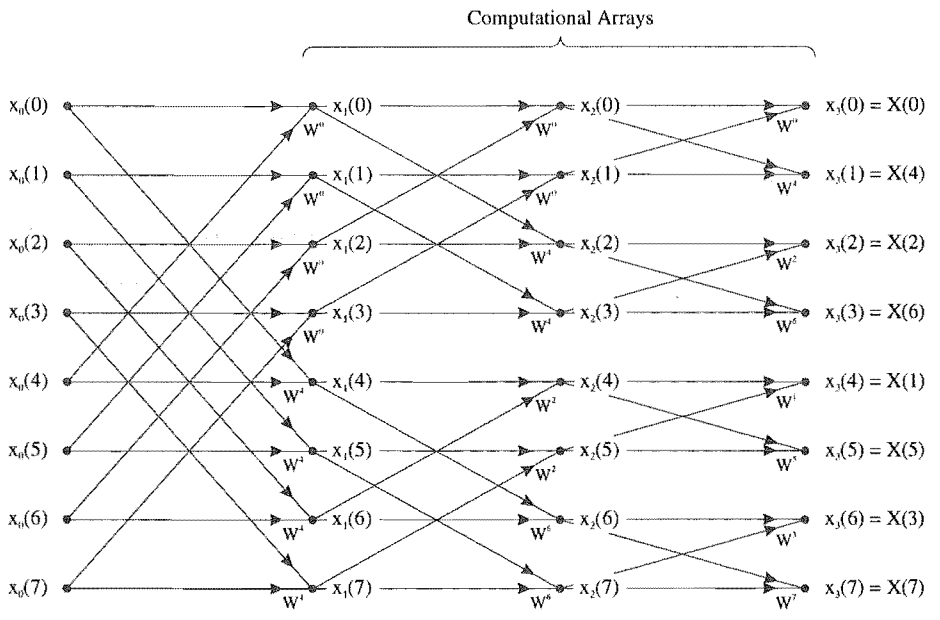

Figure 5.11 DIT FFT signal flow graph for N = 8

$$
\begin{aligned}
x_1(0,0,0) &= x_0(0,0,0) + x_0(1,0,0)W^0 \\
x_1(0,0,1) &= x_0(0,0,1) + x_0(1,0,1)W^0 \\
x_1(0,1,0) &= x_0(0,1,0) + x_0(1,1,0)W^0 \\
x_1(0,1,1) &= x_0(0,1,1) + x_0(1,1,1)W^0 \\
x_1(1,0,0) &= x_0(0,0,0) + x_0(1,0,0)W^4 \\
x_1(1,0,1) &= x_0(0,0,1) + x_0(1,0,1)W^4 \\
x_1(1,1,0) &= x_0(0,1,0) + x_0(1,1,0)W^4 \\
x_1(1,1,1) &= x_0(0,1,1) + x_0(1,1,1)W^4
\end{aligned}
\qquad (5.47)
$$

which are used to construct the first computational array in Figure 5.11. Enumerating the remaining summations in Eqs. (5.44) in the same way leads to equation sets that allow the rest of the signal flow graph to be constructed.

Inspection the last equation in Eqs. (5.44) shows that the output data is in bit reversed order as is also shown in Figure 5.11. A bit reversing procedure is required to rearrange the output data into the correct order. Furthermore it can be demonstrated that bit reversing is needed to determine the powers of W in Figure 5.11. To avoid having to perform the later bit reversing operations in software the TICMS design uses an FFT implementation in which the input data is bit reversed (see 5.5.3) prior to being transformed into the frequency domain. As a result of this the powers of W and the output occur in natural order as shown in the modified signal flow graph in Figure 5.12, which is obtained from Figure 5.11 by bit reversing the input data and the nodes in all computational arrays in such a way that the transmission paths in Figure 5.11 are maintained. The arrays in Figure 5.12 have been relabeled so that each node index corresponds to the node's vertical position in the array as this facilitates the development of an FFT software algorithm.

The modified signal flow graph in Figure 5.12 forms the basis for the FFT implementation used in the TICMS design and is used to develop an FFT software algorithm for any N that is a power of 2. Inspection of Figure 5.12 shows that in every array it is possible to find two nodes whose input transmission paths stem from the same pair of nodes in the previous array, for example nodes $y_2(0)$ and $y_2(2)$ are computed in terms of nodes $y_1(0)$ and $y_1(2)$. Two such nodes are referred to as a dual node pair as indicated in Figure 5.12. Since the computation of a dual node pair is independent of other nodes then it is possible to perform in-place computation, where for example $y_3(1)$ and $y_3(5)$ are computed in terms of $y_2(1)$ and $y_2(5)$ and the results returned to the storage locations occupied by $y_2(1)$ and $y_2(5)$. Hence the storage requirements for the algorithm are limited to the input data array size, an important property as TICMS design uses a 2048 point FFT.

Inspection of Figure 5.12 reveals the spacing between dual nodes in array i is given by

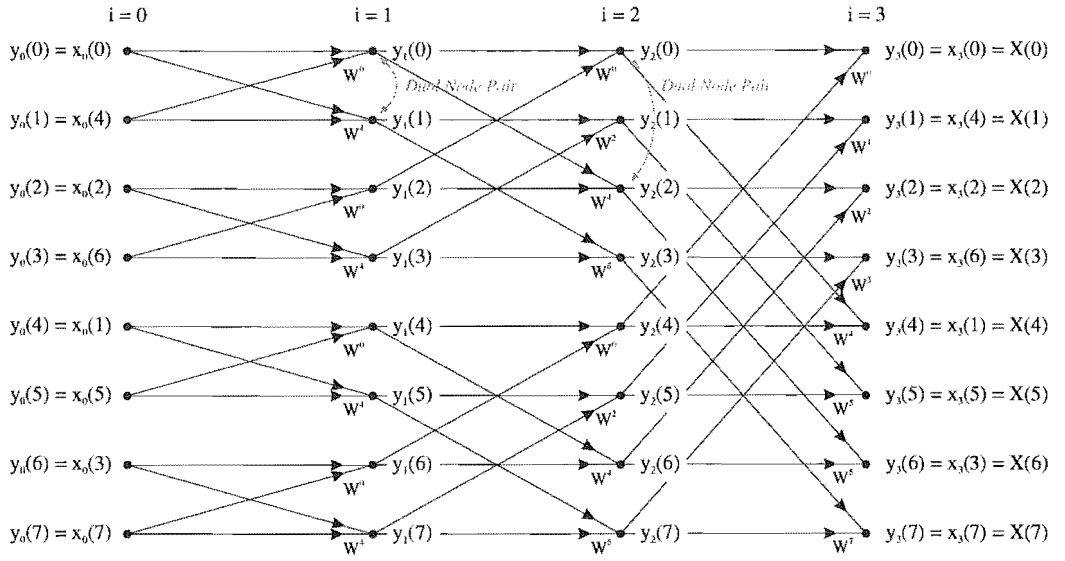

Figure 5.12 Modified signal flow graph for the case N = 8

$$\text{Dual Node Spacing} = 2^{i-1} \tag{5.48}$$

so that the dual node of $y_i(k)$ is $y_i(k + 2^{i-1})$. Referring again to Figure 5.12 it is seen that each dual node pair can be computed as follows

$$\begin{aligned} y_i(k) &= y_{i-1}(k) + W^p y_{i-1}(k+2^{i-1}) \\ y_i(k+2^{i-1}) &= y_{i-1}(k) + W^{p+N/2} y_{i-1}(k+2^{i-1}) \end{aligned} \tag{5.49}$$

which is simplified to

$$\begin{aligned} y_i(k) &= y_{i-1}(k) + W^p y_{i-1}(k+2^{i-1}) \\ y_i(k+2^{i-1}) &= y_{i-1}(k) - W^p y_{i-1}(k+2^{i-1}) \end{aligned} \tag{5.50}$$

since

$$W^{p+N/2} = W^p(e^{(-j2\pi/N)(N/2)}) = -W^p \tag{5.51}$$

Before dual nodes can be computed it is necessary to determine the power of W in Eqs. (5.50). By further inspecting Figure 5.12 it is easily shown that

$$p = (k.2^{\gamma-i}) \bmod N \tag{5.52}$$

For example for node $y_1(3)$ p = 4 as verified in Figure 5.12.

The DAPM DSP FFT software module determines the FFT of the input sequence by computing each computational array starting from i = 1 and proceeding until i = γ. Each

computational array is computed by starting at node k = 0 and sequentially working down the array computing Eqs. (5.50). Because the dual node spacing is 2^{i-1} then 2^{i-1} nodes must be skipped after every 2^{i-1}th node. To clarify this consider array i = 2 in Figure 5.12 for which the dual node spacing is 2. Because nodes $y_2(2)$ and $y_2(3)$ are the duals of nodes $y_2(0)$ and $y_2(1)$ then they are computed along with $y_2(0)$ and $y_2(1)$ according to Eqs. (5.50). Therefore when proceeding down the array it is necessary to skip nodes $y_2(2)$ and $y_2(3)$ as they have already been computed. In summary to compute array i the FFT module computes the first 2^{i-1} nodes, skips the next 2^{i-1} nodes continuing until a node index greater than N-1 is reached. Further details on the FFT software module can be found in 6.2.4.

5.5.3 Bit Reversing

A binary number is said to be the bit reverse of a second when its bits are obtained by mirroring those of the second about an imaginary mirror line drawn between the two. For example 1010 is said to be the bit reverse of 0101. As has already been discussed it is necessary to bit reverse the input data array for the FFT algorithm used in the TICMS design. This is accomplished by exchanging $x_0(k)$ and $x_0(j)$ where j is obtained by bit reversing k.

To illustrate the bit reversing procedure used in the TICMS design, consider a number N that is represented in binary as $b_4b_3b_2b_1$. To bit reverse N first each b_i is determined. To determine b_1, N is divided by 2 and truncated which is equivalent to shifting the binary representation one bit to the right to obtain $b_4b_3b_2$. This result is then multiplied by 2 and subtracted from N to determine b_1 as follows

$$b_1 = b_4b_3b_2b_1 - 2.b_4b_3b_2 = b_4b_3b_2b_1 - b_4b_3b_20 \tag{5.53}$$

Next b_2 is determined in the same way by dividing $b_4b_3b_2$ by 2. After all b_i have been determined the bit reversed number is determined as follows

$$N_{BitReversed} = b_1.2^3 + b_2.2^2 + b_3.2^1 + b_4.2^0 \tag{5.54}$$

Further software details can be found in 6.2.4.

5.5.4 FFT of Two Signals Simultaneously

The TICMS DSP application software is able to transform the voltage and current channel time domain data into the frequency domain simultaneously by forming a complex time function as detailed below. As a result of this large computational savings are possible as the 2048 point FFT algorithm doesn't have to be called a second time. This optimisation is possible as the voltage and current channel time domain signals are real-valued whereas the

radix-2 DIT FFT algorithm just described, in general accepts a complex input as follows

$$X(k) = \frac{1}{N}\sum_{n=0}^{N-1}[x_r(n) + jx_i(n)]W^{nk} \quad k = 0, 1, \ldots, N-1 \tag{5.55}$$

Rather than optimise the FFT algorithm for real data, the complex time function approach was used so that the same code could be used to perform an inverse DFT (IDFT) on a frequency domain signal, which is in general complex. It is easily shown that the IDFT is obtained by taking the DFT of the complex conjugate of the frequency domain signal and then taking the complex conjugate of the result as follows

$$x(n) = \frac{1}{N}\left[\sum_{k=0}^{N-1}[X_r(k) + jX_i(k)]^* W^{nk}\right]^* \quad n = 0, 1, \ldots, N-1 \tag{5.56}$$

This dual nature of the FFT code allows the IDFT to be easily included in future DSP software modifications.

When transforming the real-valued signals captured by the TICMS it is necessary to set the imaginary part in Eq. (5.55) to zero. However this approach is inefficient as the multiplications involving $jx_i(n)$ are still performed in software even though it is zero. To avoid this inefficiency the TICMS design forms a complex time domain function with the real and imaginary parts set as follows

$$x(n) = v_{in}(n) + jv_{out}(n) \tag{5.57}$$

where $v_{in}(n)$ and $v_{out}(n)$ represent the sampled voltage and current channel signals respectively. Because the DFT is a linear operation the DFT of Eq. (5.57) can be expressed as follows

$$\begin{aligned} X(k) &= V_{in}(k) + jV_{out}(k) \\ &= [V_{in(r)}(k) + jV_{in(i)}(k)] + j[V_{out(r)}(k) + jV_{out(i)}(k)] \\ &= [V_{in(r)}(k) - V_{out(i)}(k)] + j[V_{in(i)}(k) + V_{out(r)}(k)] \\ &= X_r(k) + jX_i(k) \end{aligned} \tag{5.58}$$

where $X_r(k)$ and $X_i(k)$ are output by the FFT algorithm. To see how $V_{in}(k)$ and $V_{out}(k)$ are extracted from X(k) it is useful to write X(k) as follows

$$X(k) = \frac{1}{N}\sum_{n=0}^{N-1}\left[v_{in}(n) + jv_{out}(n)\right]e^{-j2\pi nk/N} \tag{5.59}$$

which is simplified to produce

$$X(k) = \frac{1}{N}\sum_{n=0}^{N-1}\left[v_{in}(n)\cos\frac{2\pi nk}{N} + v_{out}(n)\sin\frac{2\pi nk}{N}\right] + j\frac{1}{N}\sum_{n=0}^{N-1}\left[v_{out}(n)\cos\frac{2\pi nk}{N} - v_{in}(n)\sin\frac{2\pi nk}{N}\right] \quad (5.60)$$

where each summation represents $X_r(k)$ and $X_i(k)$ from Eq. (5.58) respectively. The even and odd symmetry of the cosine and sine functions respectively allows Eq. (5.60) to put into the following form

$$X(k) = X_{r(e)}(k) + X_{r(o)}(k) + j\left[X_{i(e)}(k) + X_{i(o)}(k)\right] \quad (5.61)$$

where the e and o subscripts are used to denote even and odd components. By setting $v_{out}(n)$ to zero, Eqs. (5.58) (5.60) and (5.61) result in

$$X(k) = V_{in}(k) = X_{r(e)}(k) + jX_{i(o)}(k) \quad (5.62)$$

Similarly setting $v_{in}(n)$ to zero results in

$$X(k) = jV_{out}(k) = X_{r(o)}(k) + jX_{i(e)}(k) \quad (5.63)$$

It is easily shown that any frequency domain signal can be decomposed into even and odd components as follows

$$H(k) = H_e(k) + H_o(k) = \left(\frac{H(k)}{2} + \frac{H(N-k)}{2}\right) + \left(\frac{H(k)}{2} - \frac{H(N-k)}{2}\right) \quad (5.64)$$

Applying this decomposition to the even and odd components of $X_r(k)$ and $X_i(k)$ results in

$$X_{r(e)}(k) = \left(\frac{X_r(k)}{2} + \frac{X_r(N-k)}{2}\right) \quad (5.65)$$

$$X_{r(o)}(k) = \left(\frac{X_r(k)}{2} - \frac{X_r(N-k)}{2}\right) \quad (5.66)$$

$$X_{i(e)}(k) = \left(\frac{X_i(k)}{2} + \frac{X_i(N-k)}{2}\right) \quad (5.67)$$

and

$$X_{i(o)}(k) = \left(\frac{X_i(k)}{2} - \frac{X_i(N-k)}{2}\right) \quad (5.68)$$

Substituting Eqs. (5.65) (5.66) (5.67) and (5.68) into Eqs. (5.62) and (5.63) produces the desired results, namely

$$V_{in}(k) = \frac{X_r(k)}{2} + \frac{X_r(N-k)}{2} + j\left(\frac{X_i(k)}{2} - \frac{X_i(N-k)}{2}\right) \tag{5.69}$$

and

$$V_{out}(k) = \frac{X_i(k)}{2} + \frac{X_i(N-k)}{2} - j\left(\frac{X_r(k)}{2} - \frac{X_r(N-k)}{2}\right) \tag{5.70}$$

In summary the DSP application software performs a sorting procedure as defined by Eqs. (5.69) and (5.70) to extract $V_{in}(k)$ and $V_{out}(k)$ once the DFT of the complex time function has been determined. The computational requirements of this sorting procedure are minimal compared to calling a 2048 point FFT algorithm a second time as discussed next.

5.5.5 Computational Requirements

One complex multiplication and two complex additions are required to compute a dual node pair using Eqs. (5.50). Because the signal flow graph for $N = 2^{\gamma}$ consists of γ computational arrays then $N\gamma/2$ complex multiplications and $N\gamma$ complex additions are required to compute an N point DFT using the FFT algorithm previously described. Assuming that computing time is proportional to the number of complex multiplications then the ratio of direct DFT to FFT computing time is given as

$$\frac{N^2}{N\gamma/2} = \frac{2N}{\gamma} \tag{5.71}$$

which for N = 2048 is a computational reduction of 372 to 1.

As discussed above a sorting procedure is required to extract the individual spectra when computing the FFT of two real signals simultaneously. Because of the symmetry present in Eqs. (5.69) and (5.70) then each need only be calculated for k = 0 to N/2 as the results for $k = (N/2)+1$ to $N-1$ are identical to those from $k = 1$ to $(N/2)-1$. Therefore each equation need only be calculated $(N/2)+1$ times. As there are two complex additions to each equation then the total number of complex additions for the sorting procedure is calculated as follows

$$\text{Complex Additions} = \left(\frac{N}{2} + 1\right) \cdot 2 \cdot 2 = 2N + 4 \tag{5.72}$$

Table 5.1 presents the number of operations and DSP processing time required to transform the captured time domain data into the frequency domain using three different computational methods for N = 2048. As can be seen the use of the sorting procedure results in a large saving when compared to performing a second 2048 point FFT.

The FFT processing time for the three DFT calculation methods presented in Table 5.1 is approximate in that the times don't take into consideration software overhead and the fact the FFT module is written in C and not DSP assembly language. Both of these factors combine to increase the quoted times although they are still useful for comparing the relative differences between each method. Also the time required to bit reverse the input data for the FFT implementations is not included as it is minimal compared those in Table 5.1.

	Direct DFT	**Separate FFT**	**Simultaneous FFT**
Complex Multiplications	2048·2048·2	(2048/2)·11·2	(2048/2)·11
Complex Additions	2048·2047·2	2048·11·2	2048·11 + 2·2048+4
Total MFLOPS	16.8	0.068	0.038
DSP Processing Time*	**504.5ms**	**2.0ms**	**1.1ms**

*** Based on TMS320C31 DSP's 33.3MFLOPS rating**

Table 5.1 Floating point operations for different DFT calculation methods using N = 2048

5.5.6 Polar Conversion

The results returned by the FFT algorithm used in the TICMS design are in rectangular format. Because the TICMS has been designed to determine the transadmittance function magnitude then the results need to be converted to polar format.

A four quadrant arctangent function is used in the DSP application software to determine the phase of $V_{in}(k)$ and $V_{out}(k)$. This function produces ±360° phase jumps when the imaginary part goes from negative to positive and vice versa while the real part is negative as indicated in Figure 5.13. To avoid these phase jumps it is necessary to 'unwrap' the phase by adding ∓360° to all phase angles following and including the ones with

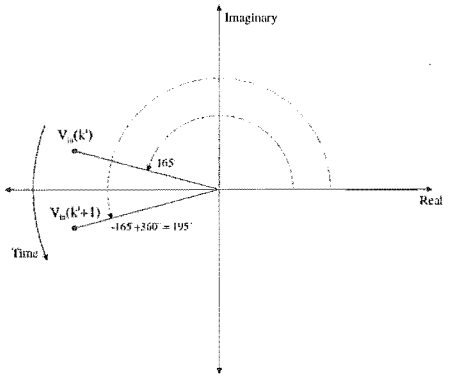

Figure 5.13 Illustrating the affect of phase jump

the $\pm 360°$ jump.

5.6 Transadmittance Function

Figure 5.14 shows the current TICMS test setup. To determine the transadmittance function of the transformer under test additional digital signal processing is required to determine the spectra of $v_{trans}(n)$ and $i_{trans}(n)$ from the digitised $v_{in}(t)$ and $v_{out}(t)$. If this additional processing is not performed then the transadmittance function of the transformer and transducers combined results.

Before $V_{trans}(k)$ can be determined $V_{imp}(k)$ must be calculated from $V_{in}(k)$. This calculation is easily formulated by treating the voltage channel transducer as a separate system as illustrated in Figure 5.15. In Appendix E it is shown that the transfer function of the voltage transducer is

$$H_2(f) = \frac{j\omega/\omega_2}{j\omega/\omega_{12}+1} = \frac{jf/f_2}{jf/f_{12}+1} \tag{5.73}$$

where

$$f_2 = \frac{1}{2\pi R_2 C} \tag{5.74}$$

and

$$f_{12} = \frac{1}{2\pi(R_1+R_2)C} \tag{5.75}$$

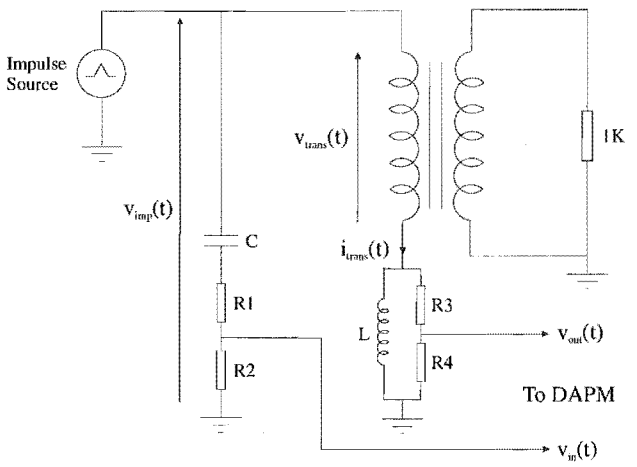

Figure 5.14 TICMS test setup

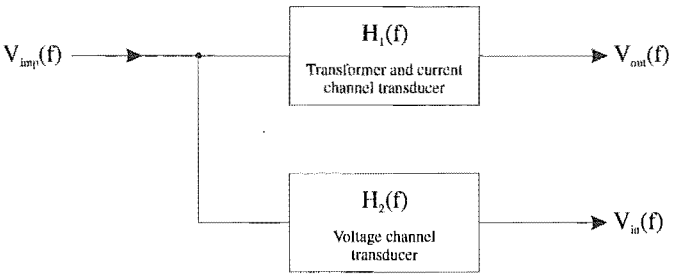

Figure 5.15 System view of transformer and transducers

From Figure 5.15 and Eq. (5.73) it is easily seen that

$$\left|V_{imp}(f)\right| = \frac{\left|V_{in}(f)\right|}{\left|H_2(f)\right|} = \frac{\left|V_{in}(f)\right|\sqrt{1+(f/f_{12})^2}}{f/f_2} \tag{5.76}$$

and

$$\Phi_{V_{imp}(f)} = \Phi_{V_{in}(f)} - \Phi_{H_2(f)} = \Phi_{V_{in}(f)} - \frac{\pi}{2} + \tan^{-1}\left(\frac{f}{f_{12}}\right) \tag{5.77}$$

By applying Eqs. (5.76) and (5.77) to each discrete frequency in $V_{in}(k)$ the DSP application software is able to determine $V_{imp}(k)$.

By summing the voltages in Figure 5.14 it is easily seen that

$$v_{trans}(t) = v_{imp}(t) - \frac{(R_3+R_4)v_{out}(t)}{R_4} \tag{5.78}$$

Applying the frequency domain equivalent of Eq. (5.78) to each discrete frequency in $V_{imp}(k)$ produces the desired result

$$V_{trans}(k) = V_{imp}(k) - \frac{(R_3+R_4)V_{out}(k)}{R_4} \tag{5.79}$$

To determine $I_{trans}(k)$ it is necessary to know the complex impedance of the RL shunt in Figure 5.14. Appendix E derives this as follows

$$Z = \frac{j\omega(R_3+R_4)/\omega_c}{1+j\omega/\omega_c} = \frac{jf(R_3+R_4)/f_c}{1+jf/f_c} \tag{5.80}$$

where

$$f_c = \frac{R_3+R_4}{2\pi L} \tag{5.81}$$

From Figure 5.14 and Eq. (5.80) $I_{trans}(f)$ is easily produced as follows

$$I_{trans}(f) = \frac{V_{out}(f)(1 + jf/f_c)}{jfR_4/f_c} \tag{5.82}$$

$I_{trans}(k)$ is then obtained by evaluating Eq. (5.82) at each discrete frequency.

Another method for determining $V_{trans}(f)$ and $I_{trans}(f)$ is to use time domain convolution to calculate $v_{trans}(t)$ and $i_{trans}(t)$ from $v_{in}(t)$ and $v_{out}(t)$. However this method requires more complex multiplications and additions as $v_{trans}(n)$ and $i_{trans}(n)$ still have to transformed into the frequency domain at the finish so that the transadmittance function can be determined.

5.6.1 Transadmittance Function Magnitude

From 3.5 the transadmittance function magnitude of the transformer in Figure 5.14 is determined as follows

$$|H_{trans}(f)| = \frac{|I_{trans}(f)|}{|V_{trans}(f)|} \tag{5.83}$$

To determine the discrete version of $|V_{trans}(f)|$ it is necessary to convert Eq. (5.79) to rectangular form as follows

$$V_{trans}(k) = |V_{imp}(k)|(\cos\alpha + j\sin\alpha) - \frac{(R_3+R_4)|V_{ont}(k)|(\cos\beta + j\sin\beta)}{R_4} \tag{5.84}$$

where

$$\alpha = \Phi_{V_{imp}(k)} \tag{5.85}$$

and

$$\beta = \Phi_{V_{out}(k)} \tag{5.86}$$

To determine $|V_{trans}(k)|$ the real and imaginary components of Eq. (5.84) are combined and the magnitude of the result taken to produce

$$|V_{trans}(k)| = \sqrt{x^2 + y^2} \tag{5.87}$$

where

$$x^2 = |V_{imp}(k)|^2 \cos^2\alpha - 2|V_{imp}(k)||V_{out}(k)|\left(\frac{R_3+R_4}{R_4}\right)\cos\alpha\cos\beta + |V_{out}(k)|^2\left(\frac{R_3+R_4}{R_4}\right)^2 \cos^2\beta \quad (5.88)$$

and

$$y^2 = |V_{imp}(k)|^2 \sin^2\alpha - 2|V_{imp}(k)||V_{out}(k)|\left(\frac{R_3+R_4}{R_4}\right)\sin\alpha\sin\beta + |V_{out}(k)|^2\left(\frac{R_3+R_4}{R_4}\right)^2 \sin^2\beta \quad (5.89)$$

Through the use of the following trigonometric identities

$$\cos^2\alpha + \sin^2\alpha = \cos^2\beta + \sin^2\beta = 1 \quad (5.90)$$

and

$$\cos(\alpha-\beta) = \cos\alpha\cos\beta + \sin\alpha\sin\beta \quad (5.91)$$

Eq. (5.87) is reduced to

$$|V_{trans}(k)| = \sqrt{|V_{imp}(k)|^2 + |V_{out}(k)|^2\left(\frac{R_3+R_4}{R_4}\right)^2 - 2|V_{imp}(k)||V_{out}(k)|\left(\frac{R_3+R_4}{R_4}\right)\cos(\alpha-\beta)} \quad (5.92)$$

which is suitable for use in the discrete version of Eq. (5.83).

To determine $|I_{trans}(k)|$ the magnitude of the discrete version of Eq. (5.82) is taken to produce

$$|I_{trans}(k)| = \frac{|V_{out}(k)|\sqrt{1+(k/f_c)^2}}{R_4 \quad k/f_c} \quad (5.93)$$

and the DSP application software determines the transadmittance function magnitude at each discrete frequency from Eqs. (5.92) and (5.93) as follows

$$|H_{trans}(k)| = \frac{|V_{out}(k)|f_c\sqrt{1+(k/f_c)^2}/R_4k}{\sqrt{|V_{imp}(k)|^2 + |V_{out}(k)|^2\left(\frac{R_3+R_4}{R_4}\right)^2 - 2|V_{imp}(k)||V_{out}(k)|\left(\frac{R_3+R_4}{R_4}\right)\cos(\alpha-\beta)}} \quad (5.94)$$

5.6.2 Transadmittance Function Phase

As described in 3.5 the transadmittance function phase of the transformer in Figure 5.14 is evaluated as follows

$$\Phi_{H_{trans}(f)} = \Phi_{I_{trans}(f)} - \Phi_{V_{trans}(f)} \tag{5.95}$$

To determine the discrete version of $\Phi_{V_{trans}(f)}$ the real and imaginary components of Eq. (5.84) are combined and the phase of the result taken to produce to produce

$$\Phi_{V_{trans}(k)} = \tan^{-1}\left(\frac{|V_{imp}(k)|\sin\alpha - |V_{out}(k)|((R_3+R_4)/R_4)\sin\beta}{|V_{imp}(k)|\cos\alpha - |V_{out}(k)|((R_3+R_4)/R_4)\cos\beta}\right) \tag{5.96}$$

To evaluate $\Phi_{I_{trans}(k)}$ the phase of the discrete version of Eq. (5.82) is taken to produce

$$\Phi_{I_{trans}(k)} = \Phi_{V_{out}(k)} + \tan^{-1}\left(\frac{k}{f_c}\right) - \frac{\pi}{2} \tag{5.97}$$

and the DSP applications software evaluates the transadmittance function phase at each discrete frequency form Eqs. (5.96) and (5.97) as follows

$$\begin{aligned}\Phi_{H_{trans}(k)} = {} & \Phi_{V_{out}(k)} + \tan^{-1}\left(\frac{k}{f_c}\right) - \frac{\pi}{2} \\ & - \tan^{-1}\left(\frac{|V_{imp}(k)|\sin\alpha - |V_{out}(k)|((R_3+R_4)/R_4)\sin\beta}{|V_{imp}(k)|\cos\alpha - |V_{out}(k)|((R_3+R_4)/R_4)\cos\beta}\right)\end{aligned} \tag{5.98}$$

5.7 Averaging

Noise limits the frequency to which the transadmittance function can be determined. The noise sources present in the TICMS are

- Quantisation noise caused by the digitisation process
- ADC errors
- Time jitter caused by the sample to sample variation of the sampling time from that of an ideal uniform sampling rate
- Analog noise contributed by analog electronic components
- EMI that is coupled into the analog circuits from internal and external sources

The total system noise is obtained by combining each of the noise sources above. This noise

is combined additively with the signal being digitised so that

$$t(t) = s(t) + n(t) \tag{5.99}$$

where t(t), s(t) and n(t) represent the total signal, noise free signal and total system noise signal respectively. Furthermore because the DFT is a linear operation then the spectrum of t(t) is equal to the sum of the spectra of s(t) and n(t).

Under certain conditions n(t) is random. 'Under certain conditions' must be treated with caution as theory classifies quantisation noise as nonrandom. This is because when the same signal is acquired in exactly the same way then the same amount of quantisation error will occur at the same place in the signal. However the contribution of the remaining noise sources above often injects enough randomness so that the total system noise is random. Furthermore for the TICMS, variations in the impulse produced by the IGM also helps to randomise the noise.

Random noise has an average value that tends to zero in the long term. This allows the noise level in repetitive signals to be reduced through the use of signal averaging. Signal averaging is accomplished by acquiring a repetitive signal a number of times, adding all acquisitions together and then dividing the final sum by the number of acquisitions. It is important that signal averaging be done on a DSP or μP that has more resolution (less quantisation error) than the digitiser being used. This is the case for the TICMS where a 32-bit DSP is being used to average the output of 12-bit ADCs.

Because the added noise has zero mean then its level is reduced by signal averaging. The improvement in SNR gained by signal averaging is proportional to the square root of the number of acquisitions averaged. When this number is expressed as a power of two, this corresponds to 3dB improvement for each power of two. For example 32 averages can be expressed as 2^5 which corresponds to 5·3 = 15dB of improvement.

Signal averaging is applied in the TICMS design by averaging transadmittance functions determined over separate acquisitions. Signal averaging can be applied either by the DSP application software at test time or as a post processing operation on the attached PC. Signal averaging results for 2, 4, 8, 16 and 32 averages are shown in Figure 5.16.

Because averaging improves the transadmittance function at high frequencies then it allows the effect of small winding faults to be more easily detected. However because multiple acquisitions are needed then the amount of time that it takes the TICMS to detect a fault is increased. For M averages the worst case detection time is

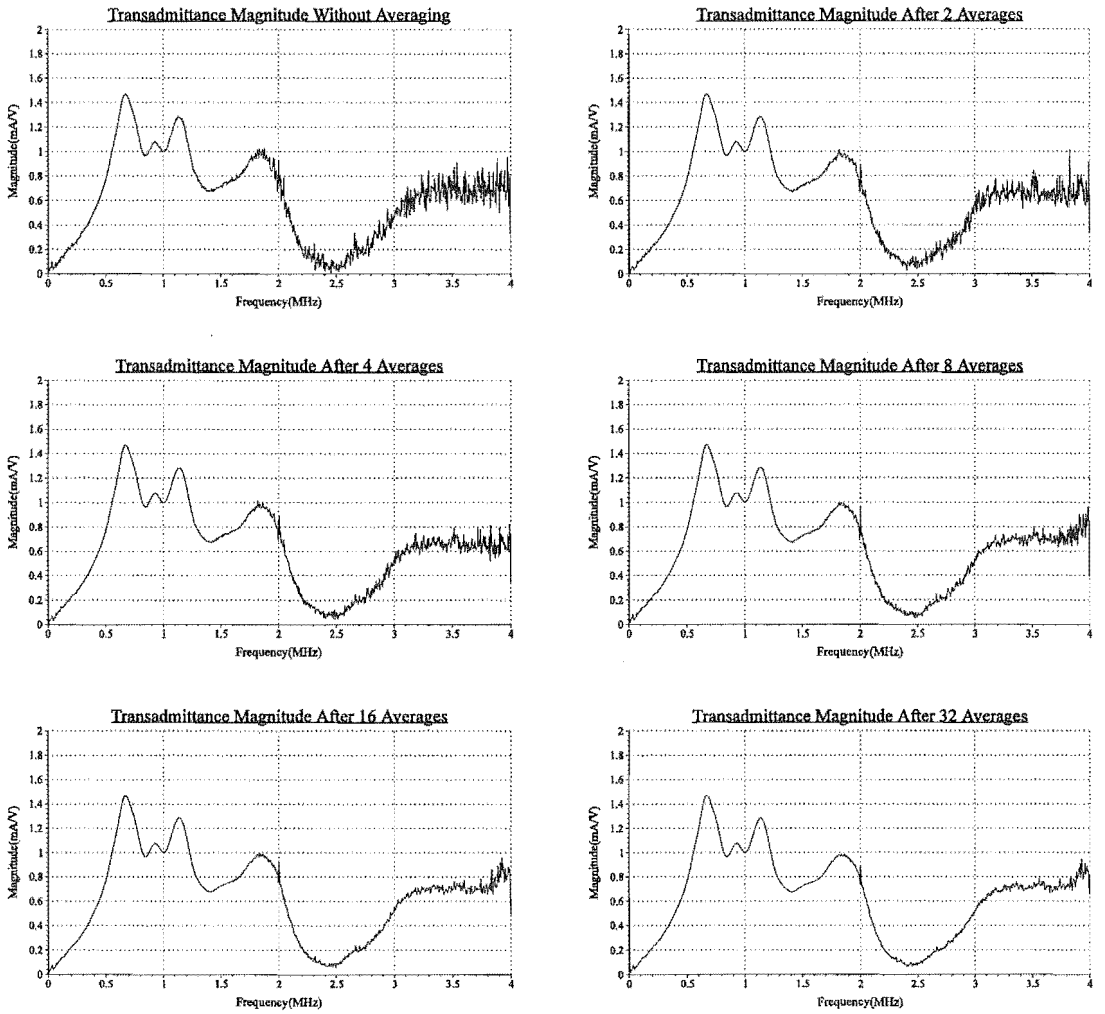

Figure 5.16 Transadmittance function averaging results

$$\text{Maximum Detection Time} = 2 \cdot M \cdot \Delta t \tag{5.100}$$

where Δt is the time taken to determine the transadmittance function once. A factor of 2 is needed in Eq. (5.100) as a fault may occur towards the end of a block of M acquisitions so that its effect is not that noticeable in the averaged result. The next averaged transadmittance function is therefore needed to fully characterise the effect of the fault.

5.8 Increasing Frequency Resolution

A consequence of using the DFT to approximate the Fourier transforms of $v_{in}(t)$ and $v_{out}(t)$ in Figure 5.14 is that the computed transadmittance function is only known at discrete frequencies. The spacing between discrete frequencies is determined from Eq. (5.23) as follows

$$\Delta f = \frac{f_s}{N} = \frac{10MHz}{2048} = 4.88kHz \qquad (5.101)$$

where f_s and N are the sampling rate and number of samples respectively. For the three transformers tested to date this resolution is sufficient to allow the transadmittance function to be represented accurately. However Δf may need to be reduced when future tests are conducted on transformers with different winding types and/or winding constructions.

A transformer transadmittance function generally consists of a series of poles that arise from internal resonances within the winding. If at a certain frequency the Q value of a pole exceeds a certain value then it is possible that a frequency resolution of 4.88kHz may not fully characterise the amplitude of a pole as shown in Figure 5.17. Worse yet if a winding fault causes the high Q pole to shift then it's amplitude may appear to change even when unaffected by the fault. This adds unwanted uncertainty into the fault evaluation process.

The above problem can be avoided by reducing Δf. This can be done by either reducing f_s or by increasing N in Eq. (5.101). Reducing f_s is not a practical option for the TICMS as it introduces aliasing errors into the system. Increasing N by appending zeros to the $v_{in}(n)$ and $v_{out}(n)$ data arrays is a solution but only at the expense of considerable additional computational time. For example reducing Δf by a factor of 8 requires that $v_{in}(n)$ and $v_{out}(n)$ be zero padded to 16384 samples which increases the number of complex multiplications and additions needed for the FFT algorithm by a factor of 20.

As a post processing operation the TICMS is able to offer a third option for reducing Δf over the band of frequencies occupied by the high Q pole. This process will be known as the zooming algorithm as it can be thought of as looking at a small window of the spectrum through a magnifying glass. Because zooming only involves time domain signal processing

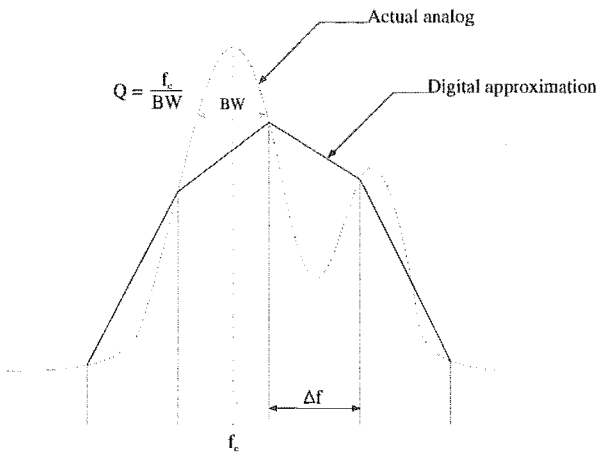

Figure 5.17 Effect of frequency resolution

techniques then it is necessary to first determine the transadmittance function at the normal Δf so that the band of frequencies over which Δf is to be reduced can be identified. Furthermore the zooming algorithm must be applied to both $v_{in}(n)$ are $v_{out}(n)$ as both are used to determine the transadmittance function.

To clarify the steps involved in the zooming algorithm it is useful to consider the test signal in Figure 5.18 where the time domain operations performed are shown on the left and their affect on the spectrum is shown on the right. The algorithm will be used to increase the resolution over the f_{BL}-f_{BH} band of frequencies occupied by the pole. First the frequency shifting property of the Fourier transform is used to shift f_{BL}-f_{BH} down to DC by multiplying by $e^{-j2\pi f_{BL}t}$ in the time domain as follows

$$g(t)e^{-j2\pi f_{BL}t} \Leftrightarrow G(f+f_{BL}) \tag{5.102}$$

A digital filter is then used to attenuate all components beyond f_{BW} where

$$f_{BW} = f_{BH} - f_{BL} \tag{5.103}$$

At design time the filter specifications are used to ensure that the filter provides at least $-\alpha_{noise}$dB of attenuation beyond f_{stop} where α_{noise} and f_{stop} represent the level of the frequency domain noise floor below ADC full-scale and the filter stopband frequency respectively. The filtered signal is then decimated so that Δf can be reduced according to Eq. (5.101). The maximum allowable decimation ratio is

$$DR_{max} = \frac{f_s/2}{f_{stop}} \tag{5.104}$$

where $f_s/2$ is the original Nyquist frequency. This can be done without aliasing errors being introduced as all frequency components of the filtered signal beyond f_{stop} are below the frequency domain noise floor as illustrated in Figure 5.18. Finally the decimated signal is zero padded to 2048 samples and transformed into the frequency domain where the resulting spectrum is equal to the original band of interest at an increased resolution. The increase in resolution possible is determined by DR_{max}. For the test signal DR_{max} is equal to 5 and from Eq. (5.101) this reduces Δf over f_{BL}-f_{BH} from 4.88kHz to 976Hz. Figure 5.18 compares the f_{BL}-f_{BH} band before and after zooming and shows that a 2dB error in the pole height was present at the lower resolution. Using zero padding to gain this improvement in resolution would involve padding to 16384 samples (the nearest power of 2 above 5·2048) which would increase the number of complex operations be a factor of 20 as previously explained.

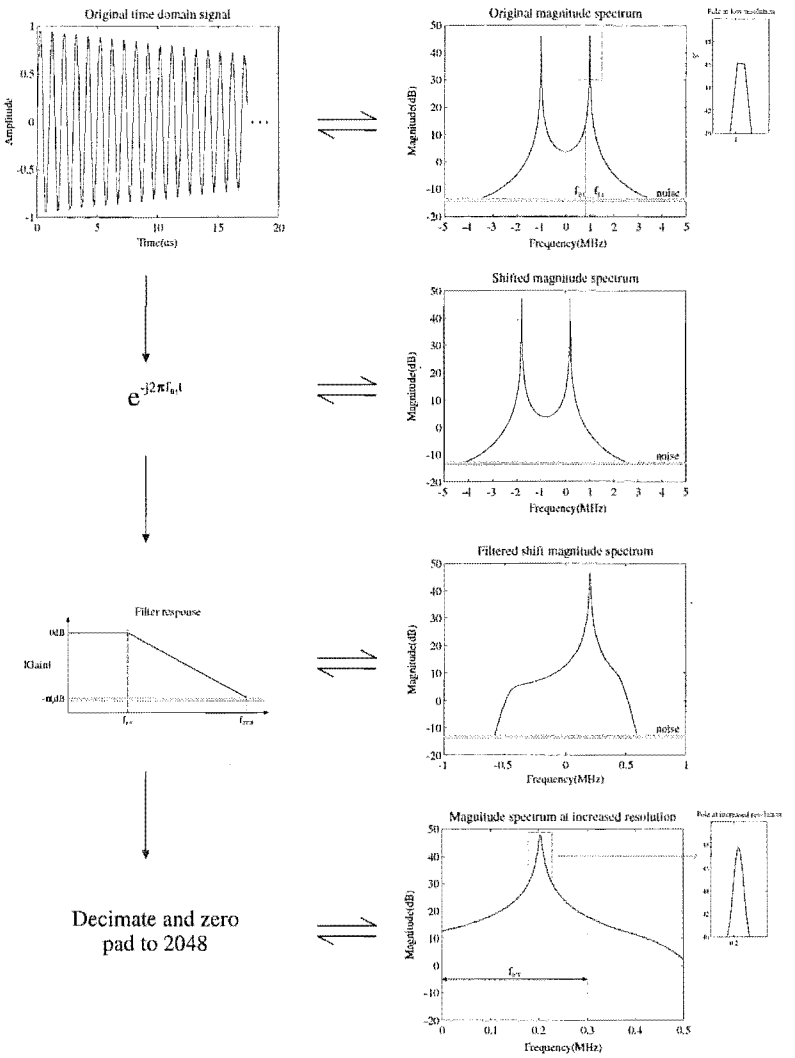

Figure 5.18 Steps involved in the zooming algorithm

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Chapter 6

SOFTWARE DESIGN

The purpose of this chapter is to describe the three software designs that have been developed for the TICMS prototype. In the first section the three software designs are introduced and an overview of the software design process used is given. The second section describes in more detail the steps involved in the development of the DAPM application software while the remaining two sections give a functional overview of the TICMS Windows application software and the DAPM diagnostic software.

6.1 Overview

The TICMS software design process involved the development of the following software systems:

- **DAPM application software:** Calculates the transadmittance function from captured time domain data received from the transient digitiser and sends the results to an attached PC.
- **TICMS Windows application software:** PC software that receives and displays processed data from the DAPM.
- **DAPM diagnostic software:** A series of software routines that test the functionality of the DAPM hardware.

During the design of these software systems the following phases were completed:

- **Requirements analysis:** Structured analysis was used for the requirements analysis phase in order to develop an implementation independent software model for the proposed system. Included in this phase were the specification of any nonfunctional requirements.
- **Preliminary design:** Structured design was used to design the software structure during the preliminary design phase. At this time the modules that comprise the system were designated and their interrelations were specified. During this design phase procedural

and data abstractions were also specified and module headers were created.

- **Detailed design:** During this design phase the contents of each module were specified and a decision was made concerning the algorithm to be used. Nassi-Shneiderman charts were used to represent the algorithm of some of the DAPM application software modules as they facilitate the development of structured code.
- **Coding and Integration:** During this phase of the design cycle the source code for each module was written. This phase also involved integrating the modules together and testing the system as modules were added.

In the following section, each of these design phases are discussed in more detail for the DAPM application software.

6.2 DAPM Application Software

The DAPM application software determines the winding transadmittance function of the transformer under test by performing digital signal processing operations on captured time domain data transferred from the transient digitiser. This process is controlled by user commands that are received from an attached PC via an asynchronous serial link. The DAPM application software decodes the received command and performs the requested test procedure. User requested results from the test procedure are then sent to the TICMS Windows application software where they are displayed and archived to the PCs HDD.

6.2.1 Requirements Analysis

In developing the DAPM application software, structured analysis was first used to formally document the software requirements. Structured analysis is most useful for traditional data processing systems were data flows among activities in the system. The DAPM application software is a good example of this type of system. A software model for the proposed system defined using structured analysis is presented in Appendix A, and consists of the following components:

- **Data-flow diagrams:** Diagrams that show activities, data stores and the flow of data within the system.
- **Data dictionary:** A list of all the data elements in the data-flow diagrams, along with a definition and description of each.
- **Activity specifications:** Descriptions of each of the activities indicated in the data-flow diagrams.

The model produced by structured analysis defines what the DAPM application software

must do, but does not specify how it is to be done. The model is therefore implementation independent and can be implemented in either a high level language such as C or in assembly language. As a consequence of this independence, the model developed may be used as a basis for all future versions of the software.

6.2.1.1 Nonfunctional Requirements

The model developed during structured analysis describes the functional requirements of the proposed system. Functional requirements describe how the system should behave given certain inputs. Nonfunctional requirements are requirements or restrictions that do not relate directly to the functions performed by the system. The following nonfunctional requirements were identified during the DAPM application software design process:

I. Hardware Considerations

- The system is to be designed to run on the TICMS DAPM.
- The system must be capable of running within 128K of DAPM RAM.
- The system is required to interface to an attached PC via an asynchronous serial communications interface so that data can be displayed and archived to HDD.

II. Performance Characteristics

- The system must be capable of determining the transadmittance function in real-time (less than 500ms).
- The system must be able to temporarily store up to 100K of data.

III. Error Handling and Extreme Conditions

- The system must be able to detect when the erroneous input data is received. This may be due to input protection circuitry being tripped or saturation at either of the ADC outputs.
- The system should not fail if the user attempts to exceed its data storage capabilities.

IV. System Interfacing

- The system receives input data from the TD in 12-bit signed 2s complement format. This must be changed to TI's 32-bit floating point format for digital signal processing calculations.
- The system output is sent to an attached PC. The output data format must be changed to IEEE single precision floating point format for compatibility with the attached PC.

V. System Modifications

- It must be easy to modify the part of the system that performs digital signal processing operations on the captured data.

- Future modifications that identify fault mechanisms are expected.

VI. Physical Environment

- The prototype target hardware will be operated in a 'noisy electronic' research laboratory that has high levels of EMI.

6.2.2 Preliminary Design

The software structure represents all of the modules in a system and their relationship to each other. Structured design was used to derive the DAPM software structure from the data-flow diagrams presented in Appendix A. Structure charts were used to represent the derived software structure as shown in Figure 6.1, where an arrow directed from module A to module B indicates that module A calls module B. Furthermore data elements that are passed from A to B during a call are labeled to the left of the arrow while those that are returned by B to A are labeled to the right. Transform analysis was used to create the structure chart by partitioning the data-flow diagrams into the following parts:

- **Afferent flow:** The activities that are associated with collecting the input data and readying it for transformation.
- **Transform center:** The activities that are concerned with transforming the input data.
- **Efferent flow:** The activities that are associated with taking the results of the transformation process and readying them for output.

This process is referred to as factoring and results in the following layer of modules being added to the structure chart of Figure 6.1 a):

- **CaptureTDData:** An afferent control module that coordinates the receipt of all incoming data and readies it for transformation.
- **CalculateTFMagPhase:** A transform control module that overseas the main processing applied to the data.
- **SendResultsToPC:** An efferent control module which coordinates all operations associated with producing the final form of the output.

Additional layers of modules were added to the structure charts in Figure 6.1 by performing further low level factoring. This low level factoring was done by expanding each of the modules produced in the preceding layer, into lower level afferent control modules and/or transform control modules and/or efferent control modules. The following design criteria were used when creating the modules in the structure chart:

- Cohesion: A module is said to be cohesive when it has a central idea or purpose and all of its components relate to performing this purpose. The DAPM application software

modules have been designed to be cohesive where each performs one clearly defined function within the system.

- Coupling: This refers to the degree of interconnectedness between modules. The DAPM application software modules were designed to be loosely coupled by limiting the number of parameters passed between modules and minimising the use of global data. Loosely coupled modules prevent bugs from propagating around the system, making the debugging process easier.
- Black boxes: A black box is a system with known input and predictable output, but whose inner workings are irrelevant. The DAPM application software modules were designed to function as black boxes.

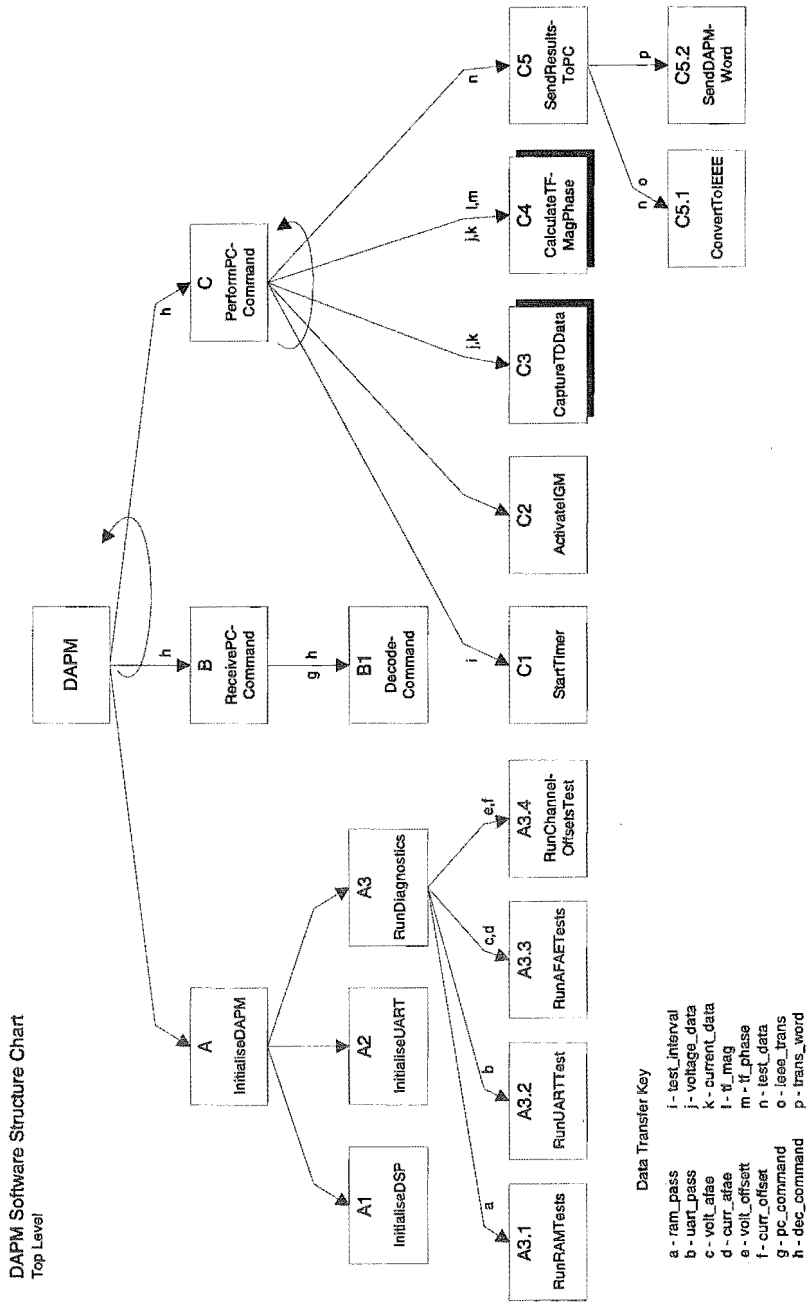


Figure 6.1 DAPM application software structure charts (a) Top level

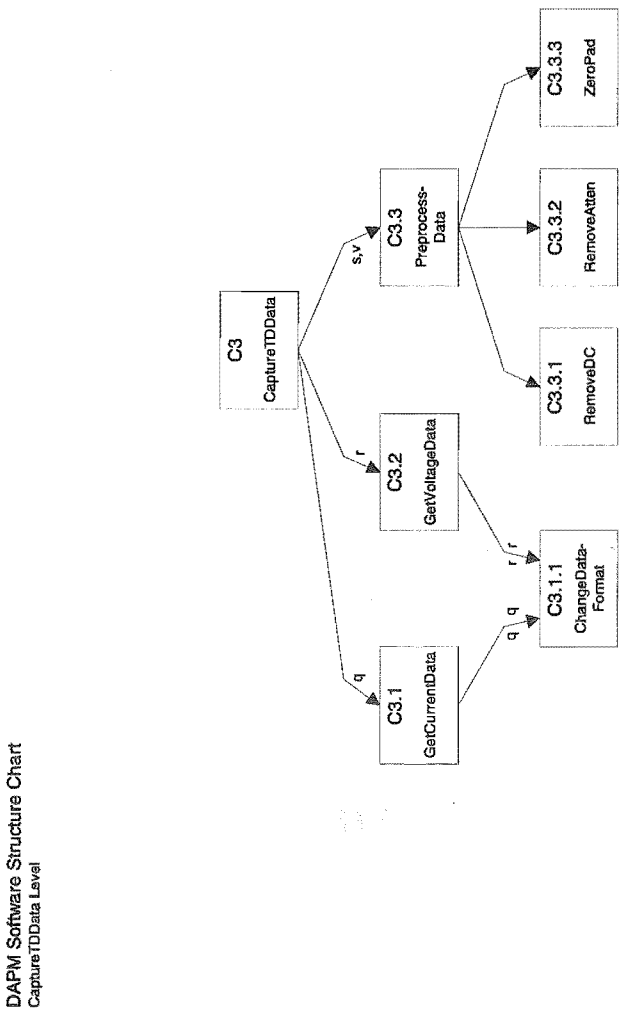


Figure 6.1 Cont. (b) CaptureTDData level

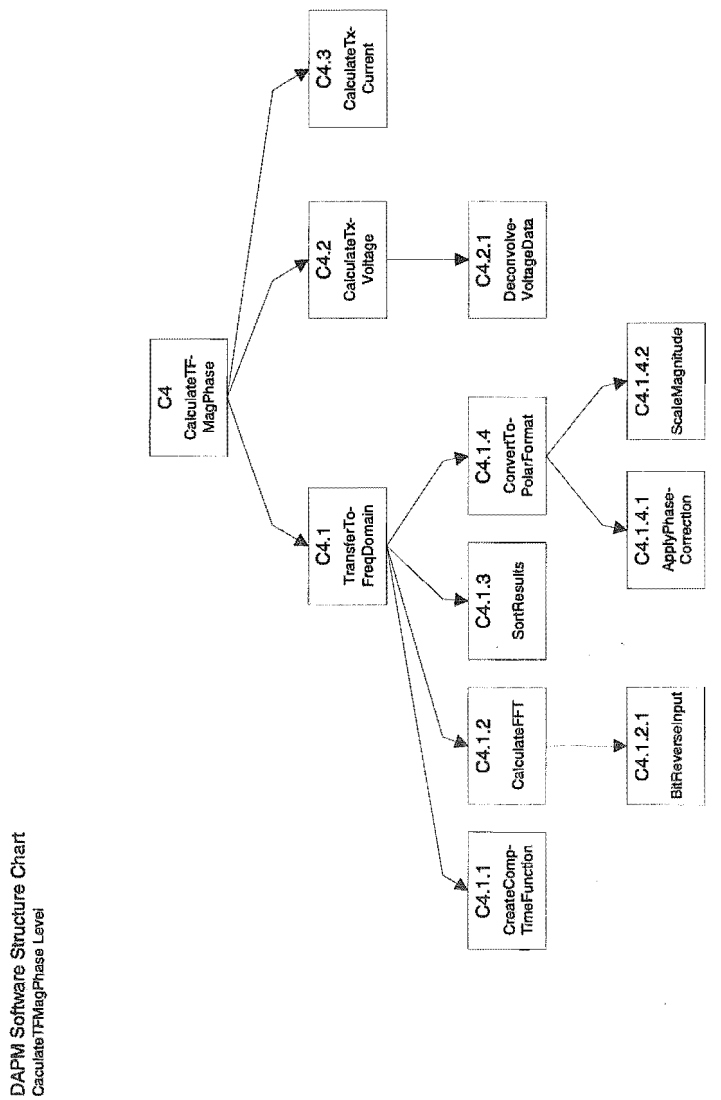


Figure 6.1 Cont. (c) CalculateTFMagPhase level

6.2.2.1 Procedural and Data Abstractions

Abstraction can be used to reduce the complexity of a problem by hiding details. During the structured design phase of the DAPM application software, procedural and data abstractions were specified where the specifications are the abstraction of the procedure or data object. Having these specifications meant that the details of a procedure or data object did not need to be examined in order to understand how to use it.

Procedural abstractions allow the target language to be extended with new operations and free the designer from any consideration of the target language. The specification of DAPM application software procedural abstractions consists of a header and a semantic part. The header consists of the procedure name and includes the number, order and type of its input and output parameters. The semantic part defines what the procedure does and consists of the following three parts:

- **Requires clause:** This states any constraints under which the abstraction is defined.
- **Modifies clause:** This lists the names of any input parameters that are modified by the procedure.
- **Effects clause:** This describes the behaviour of the procedure for all input parameters included in the requires clause.

The DAPM application software *ComplexAdd* procedural abstraction is given below. Additional DAPM application software procedural abstractions can be found in Appendix B.

ComplexAdd = **proc** (a: complex, b: complex) **returns** (sum: complex)
requires none
modifies none
effects on return the real and imaginary parts of sum are the sum of the real and imaginary parts of a and b respectively

Data abstractions allow new data types to be added to the target language without any consideration for the language to be used. The specification of DAPM application software data abstractions consists of a header, an overview section and an operations section. The header contains the name of the data type and a list of operations defined for the data type. The overview section gives an overall description of the data type while the operations section contains a specification for each operation. Each operation is specified with a procedural abstraction, as described previously. The DAPM application software *complex* data abstraction is given below.

complex = **data type is** *ComplexAdd, ComplexMult, GetReal, GetImag, SetReal, SetImag, ComplexVectorAdd, ComplexVectorMultiply*

Overview

complex consists of two ordered real numbers representing the real and imaginary parts respectively

Operations

SetReal = **proc** (a: complex, re: real)

requires none

modifies a

effects on return the real part of a is equal to re

Additional data abstractions along with the full data abstraction for *complex* (containing procedural abstractions for all defined operations) are given Appendix B for the DAPM application software.

6.2.2.2 Module Headers

A module header is a collection of comments that accompany a module in a source code listing. Module headers were created in the preliminary design of DAPM application software modules. The module header for the CalcTFMagPhase module is given below.

```
/*****************************************************************************************
  TICMS - Transformer Insulation Condition Monitoring System
  Electrical and Electronic Engineering Department
  UNIVERSITY OF CANTERBURY

  File name: TRANS.C
  Date of creation: 7/2/96
  Last updated: 9/6/97

  Title:      CalcTFMagPhase

  Purpose:    This module calculates the magnitude and phase of the
              transadmittance function from pre-processed captured time
              domain data

  Functions:  CalculateTxVoltage
              DeconvolveVoltageData
              CalculateTxCurrent
```

```
Author(s): Grant Lavery

Target system: TMS320C31 DSP of TICMS DAPM
Compiler & version: CL30 TMS320C3x C compiler, 4.50

Remarks: Compile and link project as follows:
                cl30 *.c int_vec.asm -g
                lnk30 *.obj -o ticms.out c31.cmd
*******************************************************************************/
```

6.2.3 Functional Description

A brief description of the function of the key modules identified from the structure chart follows. Descriptions of the diagnostic test modules are given in 6.3.

6.2.3.1 Command Interface Modules

The command interface modules are those that are involved with receiving command information specified by the operator of the TICMS. Because the DAPM has no user interface, the command interface modules are needed to control the operation of the DAPM. The DAPM application software contains the following command interface modules:

- **ReceivePCCommand:** Establishes a connection with the attached PC using the serial I/O handshake protocol defined in 6.4.2. Once a connection is established the command information entered by the PC operator is received.
- **DecodeCommand:** Interprets the binary command information sent over the serial interface according to a pre-defined set of rules.
- **PerformCommand:** Based upon the received command, this module controls the DAPM, activates the IGM and sequentially calls top level DAPM data capture, data processing, and data transmission modules.

6.2.3.2 Data Capture Modules

The data capture modules include those that are involved with acquiring the digitised data and readying it for transformation by the data processing modules. The DAPM application software design contains of the following data capture modules:

- **CaptureTDData:** A top level data capture module that controls the data capture and preliminary transformation process.

- **GetCurrentData:** Transfers buffered time domain samples from the current channel FIFO to DSP internal RAM and DAPM data RAM.
- **GetVoltageData:** Transfers buffered time domain samples from the voltage channel FIFO to DAPM data RAM.
- **ChangeDataFormat:** Converts captured time domain data from 12-bit 2's complement to 32-bit signed integer format and then to 32-bit TI floating-point format.
- **RemoveDC:** Subtracts the measured DC offset from the captured data for each channel. The voltage and current channel DC offset values are measured during the diagnostic test phase using offset_test after the DAPM is powered up. A description of offset_test is given in 6.3.6.
- **RemoveAtten:** Hardware attenuation is used to reduce the voltage levels of the current and voltage channel transients down to a level that is compatible with the DAPM. This module removes the effect of the hardware attenuation so that the acquired data magnitude is equal to that prior to attenuation.
- **ZeroPad:** This module zero pads the captured data so that there are 2048 samples on each channel. It is necessary to have an equal number of samples on each channel so that the frequency resolution for current and voltage channel data is the same.

6.2.3.3 Data Processing Modules

The data processing modules include those that are concerned with the main data transformation, namely calculating the transadmittance function from the acquired data. The DAPM application software design contains of the following data transformation modules:

- **CalculateTFMagPhase:** Top level data processing module that controls the main data transformation process. Calculates the magnitude and phase of the transadmittance function of the transformer under test according to Eqs. (5.94) and (5.98).
- **TransferToFreqDomain:** A high level module that controls the process of converting data from the time domain to the frequency domain.
- **CreateCompTimeFunction:** Forms a complex array where the real and imaginary elements are equal to voltage and current channel samples respectively.
- **CalculateFFT:** Produces N samples representing the frequency domain description of the N complex samples passed as input (representing a time domain signal).
- **BitReverseInput:** Rearranges the CalculateFFT input sequence so that the CalculateFFT output is in normal (i.e. not bit-reversed) order.
- **SortResults:** Applies a transformation to the output of CalculateFFT to extract

separately the spectra of the voltage and current time domain samples.

- **ConvertToPolarFormat:** Changes the complex spectral data from rectangular to polar format.
- **ApplyPhaseCorrection:** Unwraps the phase for the voltage and current channel spectra so that it is continuous and free from 2π jumps.
- **ScaleMagnitude:** Applies 1/N scaling to the calculated spectra.
- **CalculateTxVoltage:** Calculates the magnitude and phase of the voltage across the transformer under test according to Eqs. (5.92) and (5.96).
- **DeconvolveVoltageData:** Calculates the magnitude and phase of the voltage produced by the IGM according to Eqs. (5.76) and (5.77).
- **CalculateTxCurrent:** Calculates the magnitude and phase of the current through the transformer under test according to Eqs. (5.93) and (5.97).

6.2.3.4 Data Transmission Modules

The data transmission modules include those that are involved with transmitting the output data to the attached PC, and readying the processed data for output. The DAPM application software design contains of the following data transmission modules:

- **SendResultsToPC:** High level module that controls the transmission process
- **ConvertToIEEE:** Converts all data to be sent to the PC from 32-bit TI floating-point format to IEEE single precision floating-point format.
- **SendDAPMWord:** Breaks a 32-bit word into 4 bytes and transmits each over the serial interface.

6.2.4 Detailed Design

During the detailed design phase an algorithm was selected for each of the modules created by the preliminary design process. The following three guidelines were used to select an algorithm:

- Correctness: The algorithm chosen must perform the required operation correctly and in particular must not fail for negative numbers, zeros and at boundary conditions.
- Efficiency: This refers to the amount of storage and processing time expended by the algorithm. Both of these factors are important for the DAPM application software as the processing is to be done in real-time with limited primary storage available.
- Appropriateness: This refers to the appropriateness of the algorithm for the hardware

and software of the target system.

Nassi-Shneiderman charts and pseudocode were used to document the selected algorithms as both lead to the development of structured code where the flow of control is always from top to bottom, except during iteration.

The complexity or simplicity of a module is readily apparent by viewing its Nassi-Shneiderman chart. Nassi-Shneiderman charts present a more abstract view of an algorithms structure that cannot be easily seen by viewing pseudocode or even source code. Nassi-Shneiderman charts were used to document the more complex modules in the DAPM application software. The Nassi-Shneiderman chart for the CalculateFFT module is given in Figure 6.2.The level of detail used in the Nassi-Shneiderman charts was such that each chart phrase resulted in no more than 10 lines of source code.

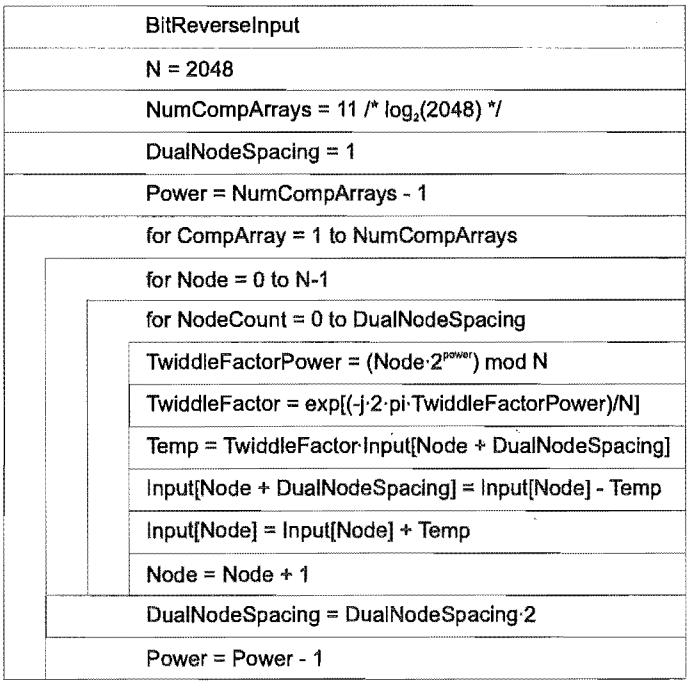


Figure 6.2 Nassi-Shneiderman chart for CalculateFFT

Pseudocode was used to document the algorithms of the simpler modules in the DAPM application software. The level of pseudocode used was more fine grained than that used in the activity specifications. The activity specification pseudocode spells out the general purpose or functions of an activity whereas the pseudocode used during the detailed design phase spells out the steps in a particular algorithm to be used.

6.2.5 Coding, Integration and Testing

During this design phase the source code for each of the modules created during the preliminary design phase was produced. The modules were then integrated together to form the DAPM application software system. As the modules were integrated, the system was tested and when integration was complete the entire system was given further testing.

An incremental integration strategy was used to code and assemble each module. This involved coding and testing some portions of the system before others and led to the entire system being created in incremental steps rather than in one monumental effort. The integration strategy used was a combination of the following:

- **Top-down method:** During this approach modules at the top of the structure chart are coded, tested and integrated first. Then modules from lower down are added until the entire system has been built.
- **Bottom-up method:** During this approach the lowest level modules in the structure chart are coded, tested and integrated first. Next higher level modules are added to form subsystems where the creation of a subsystem is called a build.
- **Threads method:** During this approach a minimal set of modules that perform some function are coded, tested and integrated. This set is called a thread and usually involves modules from different levels in the structure chart. Separate threads are formed in parallel which are then integrated to build the entire system.

When integrating the DAPM application software, the bottom-up integration method was first used to code, test and integrate the following modules:

- RunRAMTests
- RunUARTTest
- RunAFAETests
- RunChannelOffsetTest
- RunDiagnosticTests

This approach was necessary as the system was designed to run on prototype target hardware that had not been tested. Next the bottom-up method was used to add the following initialisation modules:

- InitialiseDSP
- InitialiseUART
- InitialiseDAPM

It was necessary to perform the above build at this time so that the DAPM was in a state that allowed additional application software to be coded, integrated and tested. The threads method was then used to form ReceivePCCommand and PerformPCCommand threads. As the PerformPCCommand thread was formed, the following threads were coded, integrated and tested in turn:

- CaptureTDData thread
- CalculateTFMagPhase thread
- SendResultsToPC thread

The top-down approach was used code, integrate and test each of these threads.

Different levels of testing were used as the system was coded and integrated. Digital signal processing modules were coded and unit tested in MATLAB prior to being integrated. This approach to unit testing was used as it was quick and required little test harness software to be written. Following unit testing, integration testing was performed where the system was tested after each module had been added. This testing procedure was used as any errors produced could often be quickly located in the most recently added module.

6.3 DAPM Diagnostic Software

DAPM diagnostic software was produced to test the functionality of the main hardware interfaces of the DAPM. Initially stand-alone software was written to test and debug each interface. Much of this software was later incorporated into the DAPM application software diagnostic test modules. In the sections to follow a brief functional description is given for the following diagnostic test software:

- LED_test_1: This tests the DSP, the in-circuit emulator interface, and the RAM interface and was used to test the DAPM prototype after construction.
- LED_test_2: This tests the interrupt structure when the DSP boots from EPROM and whether the development tools are being used correctly. It was used when producing an EPROM bootable version of the DAPM application software.
- Data_test: This tests the data bus of the RAM interface and was used to test the DAPM prototype after construction. It is also used during the DAPM startup sequence.
- Address_test: This tests the address bus of the RAM interface and was used to test the DAPM prototype after construction. It is also used during the DAPM startup sequence.
- AFAE_test: This tests to see if the FIFO AF/AE offset vectors were programmed correctly. It was used to test the DAPM prototype after construction and is used during

the DAPM startup sequence.

- Offset_test: This determines the amount of DC offset present on both channels of the DAPM. It is used during the DAPM startup sequence and the results are used to remove any offset of the acquired transients.
- ENOBs_test: This determines the effective number of bits of the TD and was used to test the DAPM prototype after construction.
- UART_test: This tests the UART interface and the UART's interrupt structure. It was used to test the DAPM prototype after construction and is used during the DAPM startup sequence.

6.3.1 LED Tests

LED_test_1 flashes a green LED attached to the XF0 I/O pin of the DSP. This test verified that the DSP was functioning and that the in-circuit emulator-DSP interface was working correctly. Because the in-circuit emulator transferred the program code to DAPM RAM and ran it from there, then this test also verified that the RAM interface was working. LED_test_1 cycles through all wait-states and the flash rate of the LED increases as the number of wait-states is reduced. This was used to verify that the RAM interface is capable of running with zero wait-states.

LED_test_2 was used to test the DSP interrupt structure and correct use of the development tools when booting from EPROM. To accomplish this, LED_test_2 flashes the green LED for approximately 10s and then initiates an interrupt through software. The ISR then flashes a red LED attached to another I/O pin of the DSP for approximately 10s. When the ISR returns both LEDs are flashed continuously. This tested the dual-vectoring scheme used by the DSP when booting from EPROM.

6.3.2 RAM Tests

The DAPM contains four 128k x 8 RAM chips that are organised to give 128k x 32 of DAPM RAM as shown in Figure 6.3. Two test routines, data_test and address_test, were both used to test if this RAM interface was operating correctly.

Data_test was implemented using a 32-bit moving one test. This consisted of first initializing locations 0x0 to 0x1F to zero and then writing 0x1 to location 0x0, 0x2 to location 0x1, ..., and 0x80000000 to location 0x1F. Each of these locations was then read and the results compared with what was just written. If in applying this procedure, a zero was read from any location, then the location address immediately identified the faulty bit

in the data bus. Because of the RAM organisation in Figure 6.3, then the entire data bus was tested by writing to the first 32 locations.

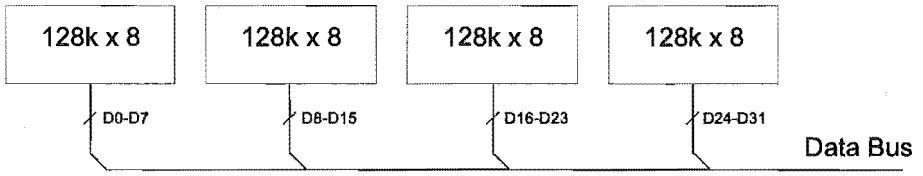


Figure 6.3 DAPM RAM organisation

Before running address_test all 128k of RAM locations were first initialised to zero. Address_test consisted of the following steps

- Performing a dummy read to location 0xFFFFFFFF, writing 0x5 to location 0x0 and then reading locations 0x1, 0x2, 0x4, ..., 0x40000000, and 0x80000000 to make sure that they were zero. Passing this phase of the test verified that the DSP could drive each address line from high to low when writing to 0x0. If in applying this procedure, 0x5 was read from any location other than 0x0, then the location address identified the address bit that the DSP was not driving low. The 0xFFFFFFFF read and 0x0 write assembly language instructions were consecutive to ensure that the write bus cycle immediately followed the read, thus causing all address bits to toggle. 0x0 was zeroed before the following phase of address_test started.
- Performing a dummy read to location 0x0, writing 0xA to location 0xFFFFFFFF and then reading 0x7FFFFFFF, 0xBFFFFFFF, 0xDFFFFFFF, ..., 0xFFFFFFFD, and 0xFFFFFFFE to make sure that they were all zero. Passing this test verified that the DSP could drive each address line from low to high when writing to 0xFFFFFFFF. If in applying this procedure 0xA was read from any location other than 0xFFFFFFFF, then the location address identified the address bit that the DSP was not driving high. The 0x0 read and 0xFFFFFFFF write assembly language instructions were consecutive to ensure that the write bus cycle immediately followed the read, thus causing all address bits to toggle.

Completing address_test successfully verified that the DSP could drive each address line either high or low.

When testing the prototype after construction, both data_test and address_test were run from DSP internal RAM to ensure that they were executing correctly and did not crash the if there was a RAM interface problem. Test results were reported using the TMS320C31 in-circuit emulator.

6.3.3 AFAE Test

After the DAPM is powered up, AFAE_test determines the voltage and current FIFO AF/AE offset vectors to make sure that they were programmed correctly at startup. AF/AE_test operates by counting the number of WRTCLK strobes received by each FIFO from the time that it was reset until the time that its AF/AE flag goes from high to low. AF/AE_test implementation involves starting Timer 1 after the TD reset interrupt is received, and then continually polling the AF/AE flag (connected to DSP XF1 input) for a change of state. When such a change is detected then the timer is stopped and the AF/AE offset vector is read from it's count register. When AF/AE_test is run the measured vectors are approximately 2 or 3 counts larger than the programmed values (32 for voltage and 64 for current). The difference is due to the time that it takes the software to turn off the timer after the polling loop detects a change in the AF/AE state. Additional FIFO details can be found in 4.8.2. The FPGA hardware used to support these tests is given in Appendix J.

6.3.4 UART Test

Whenever the DAPM is powered up or the user depresses the DAPM master reset button, the UART receives a hardware reset and all internal registers are put into a known, defined state. The first phase of UART_test reads all UART internal registers and compares the contents with the reset values given in the device data sheet. Successful completion of this phase indicates that the UART has been successfully reset. The second phase of UART_test consists of writing a test byte to each writable internal UART register and reading the register to verify that it was programmed correctly. This phase is needed as the UART interface bus cycle differs from the RAM interface bus cycle. The third phase of UART_test involves the following

- Putting the DAPM 16550 UART into loopback mode which internally connects the output of the transmitter shift register to the input of the receiver shift register so that data written to the transmitter register appears immediately at the receiver register.
- Enabling the RxRDY UART interrupt and DSP interrupt $\overline{\text{INT3}}$ (the UART interrupt, see 4.9.1.6)
- Transmitting a sequence of bytes which causes a RxRDY interrupt to be generated. The activated ISR reads the received serial sequence and compares it with what was transmitted.

6.3.5 ENOBs Test

ENOBs_test was used after DAPM construction and TICMS Windows application development to determine the effective number of bits with which the voltage channel ADC

was converting. ENOBs_test requires that the IGM be connected to the DAPM and performs the following sequence of steps

- Activates the IGM, causing the generated impulse to appear at the voltage channel analog input
- Acquires the impulse, transforms it into the frequency domain using the FFT, and puts the result into polar format
- Sends the voltage channel magnitude spectrum to the attached PC where it is appears in a display window as shown in Figure 6.4. The level of the noise floor below the full scale input voltage range is read from the display window and the ENOBs is calculated from Eq. (5.12).

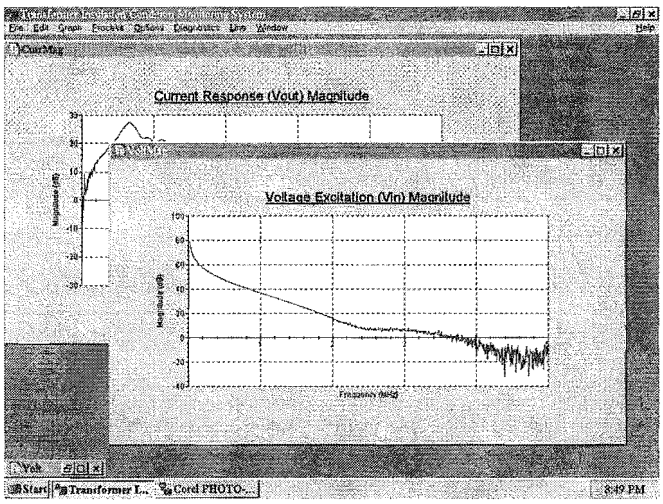


Figure 6.4 Display window used in calculating the ENOBs

The display in Figure 6.4 was captured during a typical transadmittance function test and therefore also includes the results of the inverse high pass filter processing used to increase the effective dynamic range of the system. When running ENOBs_test inverse high pass filter processing is not used so, thus giving the ENOBs of the voltage channel and not the effective system dynamic range. Further, when running ENOBs_test, care must be taken to ensure that the full scale input voltage range of the ADC is occupied if the ENOBs test is to accurate. A smaller input voltage results in smaller ENOBs result, making the system look worse than it is. For the current system configuration, ENOBs_test results in a noise floor that is -54dB below full scale, resulting in an ENOBs of

$$\text{ENOBs} = \frac{54 - 1.76}{6.02} = 8.7 \tag{6.1}$$

Because the unipolar input impulse only takes up half of the bipolar voltage range, then one bit is lost automatically. Eq. (6.1) includes the loss of this bit. A bipolar test signal was not

used as the voltage input during a typical transadmittance function test is essentially unipolar as shown in Figure 6.5 b). Because the current channel input shown in Figure 6.5 b) is bipolar, a higher ENOBs will result on the current channel during a typical test. The result of the ENOBs test can be found in paper 2 in Appendix H.

The ENOBs test will be useful for evaluating the effectiveness of noise shielding techniques. The result in Eq. (6.1) was measured with the DAPM sitting on a bench in a 'noisy' electronics lab without any shielding. Adding the analog circuitry shielding roof and housing the DAPM in its metallic enclosure will increase the ENOBs. When used next to a power transformer in service, the ENOBs test will be used to decide if additional shielding procedures are required.

6.3.6 Channel Offsets Test

The analog section of the DAPM contains two pots for adjusting the DC level in each channel. For the desired FIFO AF/AE offset vectors to program correctly, it is necessary to adjust both pots so that the nine MSBs of each ADC are zero. This procedure was performed after the prototype was constructed and does not have to be repeated. Offset_test is used during the DAPM startup sequence to measure the amount of DC on each channel. Offset_test is performed when the IGM and TUT are connected to the DAPM, and reads the output of each FIFO when no transadmittance function test is in progress. The values read are the DC levels on the respective channels.

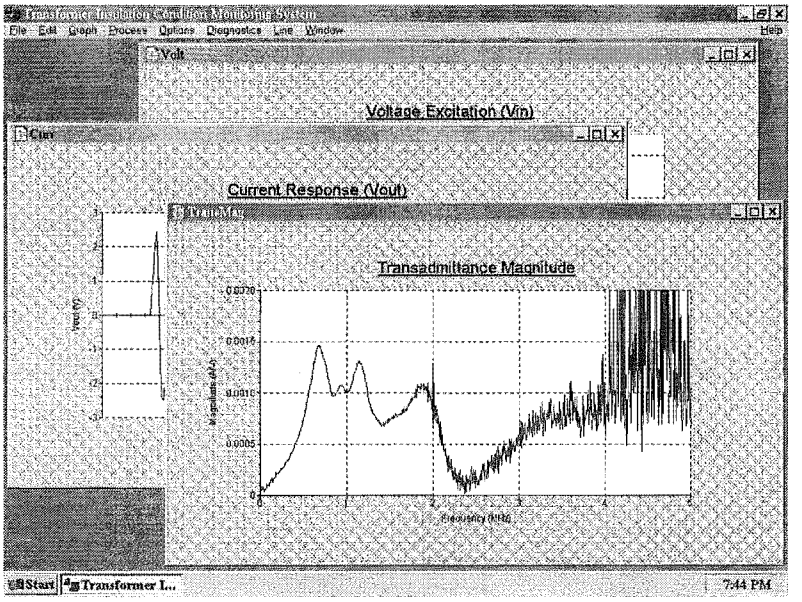
The levels returned by offset_test are used remove any DC from the acquired signals. This ensures that any DC offset differences between the two channels do not effect the transadmittance function at DC.

6.4 Windows Application Software

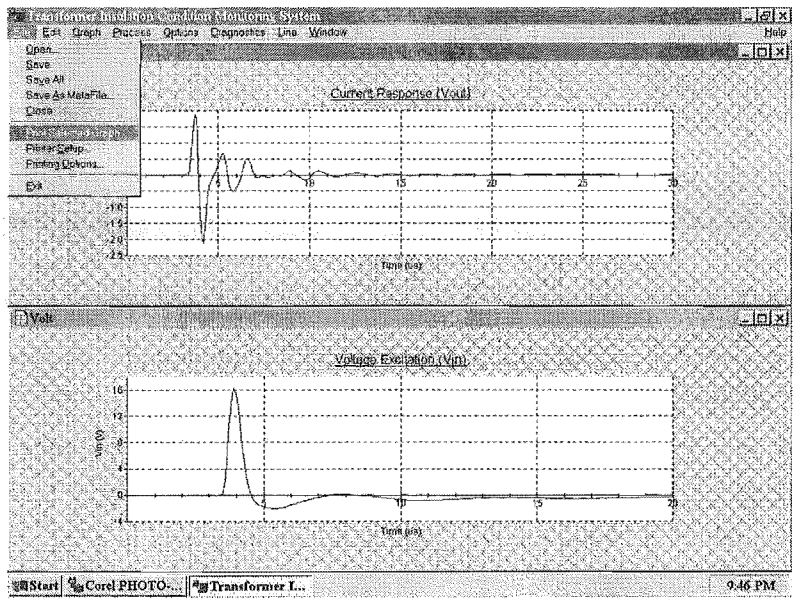
The TICMS Windows application software runs on a PC attached to the DAPM. It's purpose is to send GUI commands entered by the user to the DAPM, and to receive and display the incoming transadmittance function test data. The TICMS Windows application software requires a PC with a FIFO buffered 16550 UART. This prevents receiver overrun form occurring during high speed serial data transfers with the DAPM under Windows 95. Upon start up the TICMS application tests for the presence of a 16550, informing the user of the result.

The TICMS Windows application has been designed as a Multiple Document Interface

(MDI) application. An MDI application contains a main window called the frame window, and a number of child windows that are contained within the frame window (the parent window of the child windows). For the TICMS application, the frame window is the programs main window while the windows displaying the incoming test data (called display windows) are implemented as MDI child windows. Example screen captures of the TICMS Windows application are given in Figure 6.5. One of the advantages of an MDI application is that it allows the child windows to be arranged quickly and neatly within the parent window. This is illustrated in Figure 6.5 b), where two data windows have been tiled. Additional screen captures are included in Appendix C.



a)



b)

Figure 6.5 TICMS Windows application user interface

The TICMS application operates in one of the following two modes

- **Off-line mode:** The TICMS application starts in off-line mode. Off-line mode does not require the DAPM to be connected and is useful for re-displaying and printing previously saved test data.
- **On-line mode:** The TICMS application goes into on-line mode when the user sends a command to the DAPM. Before the command is transmitted a serial handshake protocol is used to establish a connection with the DAPM, as discussed in 6.4.2. Once a connection has been established the command is transmitted and the TICMS application waits for the DAPM to transmit the resulting test data. DAPM status LEDs are updated to inform the user that the command was received, successfully decoded, and is being performed. The TICMS application times out after a suitable period if no response is received.

6.4.1 TICMS Application Options

The TICMS application includes dialog boxes that allow the user to formulate a DAPM command, control the serial I/O port settings, control the appearance of the display windows, and to perform file I/O and printing. Each of these options are now briefly discussed.

6.4.1.1 On-Line Command Options

The TICMS application includes dialog boxes that allow the user to control on-line options. The selected on-line options are used to formulate a DAPM command, which is decoded before being performed by the DAPM. At present on-line options are available to control the following

- **Data types sent:** This option allows the user to select which of the data types produced by the DAPM are sent for display. Because the serial transmission time limits the real-time capabilities of the system (see 6.4.2 on serial I/O time), this option becomes important if the user wishes to update the display of a single data type (i.e. the transadmittance function magnitude) in real-time. Data types that can be viewed include the voltage and current channel time domain signals, the magnitude spectra of the voltage and current channels, the phase spectra of the voltage and current channels, and the magnitude and phase of the transadmittance function.
- **Graph method:** The graph method option allows the user to specify how the incoming data is to be displayed in the display window. The options for displaying new data include a new MDI child window, updating an existing display window (useful for real-

time display of a single data type), or superimposing the new data on an existing display window. The later option allows new data to be readily compared with data resulting from a previous transadmittance function test and is intended for use when a specified number of tests are performed.

- **Number tests:** Through this option the user specifies how many consecutive tests are performed when the current command is transmitted to the DAPM. Either a single test, a specified number of tests, or repeated testing can be performed. The repeated testing option is convenient when the transadmittance function is to be monitored continuously for change while the TUT is connected in service. Testing the TUT while in service is discussed in more detail in 7.4.
- **Test interval:** The test interval option allows the user to control the time interval between each transadmittance function test when either a specified number of tests or repeated testing is requested. After the DAPM application software has decoded the on-line command, the test interval is used to control the time interval between the application of consecutive impulses from the IGM.
- **Capture data before processing and sending:** This option allows the DAPM to capture all data for the requested number of tests prior to processing and transmitting the data to the PC. After data acquisition is completed, all raw data is processed and transmitted in one batch. This option is useful when it is desired to perform transadmittance function tests spaced less than 300ms apart (see Eq. (6.4)). The DAPM contains 128K of RAM, of which 10K is reserved for program storage, thus allowing up to 110 tests to be performed in this mode (see 6.4.2).

The on-line command options available in the TICMS application are illustrated in Figure 6.6. A proposed future upgrade will involve the addition of the following on-line command options

- **Data compression:** This option will enable data compression of the serial transmitted data and will allow the system to display more than one or two data types in real-time when continuous testing is employed. Lepel-Ziff compression algorithms are being investigated.
- **DSP code download:** This enhancement will allow customised DAPM application code to be downloaded without having to re-program the DAPM EPROM. The EPROM will contain a monitor program used to control the DAPM UART and to activate the DAPM code after it has been downloaded. This option will make it easy to perform DAPM code modifications in the field (if needed) without having to re-program the DAPM EPROM.
- **Diagnostic test results:** This enhancement will allow the user to view the results of the

DAPM software diagnostic tests discussed in 6.3 within a window in the TICMS application. Currently the TMS320C31 in-circuit emulator is used to display the test results.

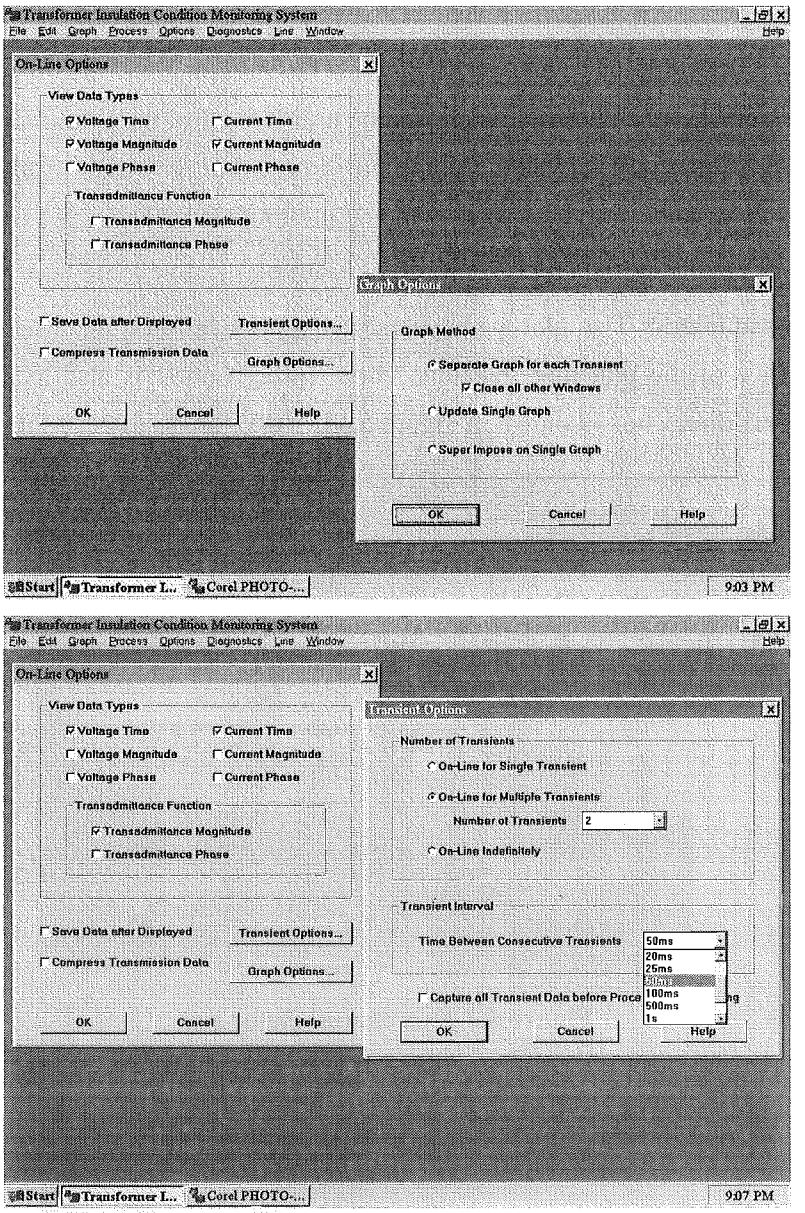


Figure 6.6 TICMS on-line command options

6.4.1.2 Display Window Options

The TICMS application includes numerous dialog boxes that contain options for customising the appearance of the display windows. Available options include

- **Axis control:** This option allows the user to control the range, step size, number of axis ticks, placement of grids, and appearance of both the vertical and horizontal axis. Logarithmic scaling can also be selected as shown in Figure 6.7.

- **Axis label control:** This option allows the user to control the appearance, position, and the number format of axis labels as shown in Figure 6.8.
- **Text size and font control:** This option allows the user to control the appearance of text used to name axis and to title graphs. The text parameters dialog box is shown in Figure 6.9.
- **Graph parameters:** This option allows the user to control the overall appearance of the graph. Available options include graph position within the window client area, size of plotting area, and colour of background and plotting areas. The graph parameters dialog box is shown in Figure 6.10.
- **Plot parameters:** The plot parameters dialog box allows the user to control the appearance of the plot line. A spline curve fitting option is also available. The plot parameters dialog box is shown in Figure 6.11.

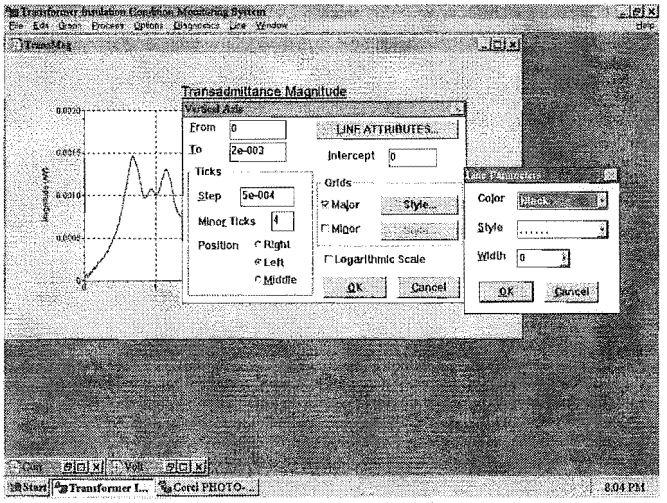


Figure 6.7 Axis control dialog box

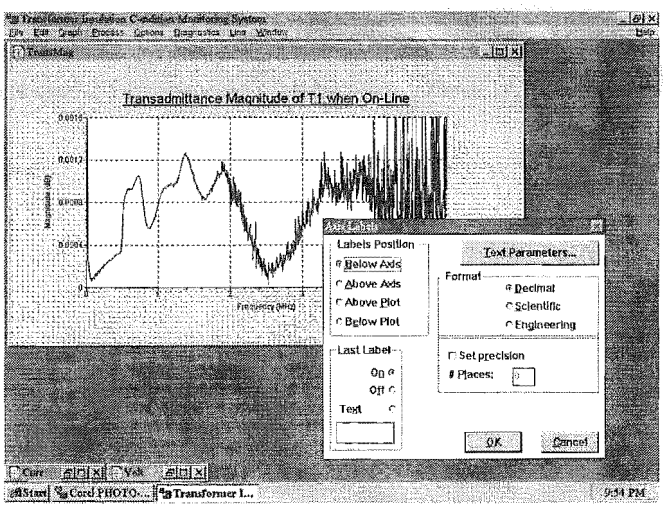


Figure 6.8 Axis label control dialog box

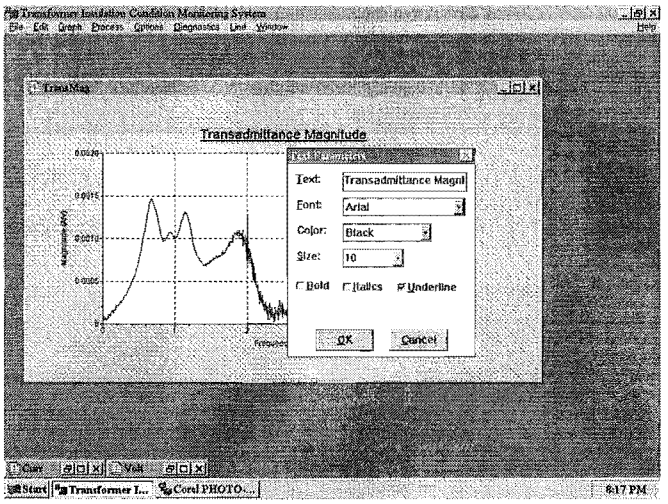


Figure 6.9 Text parameters dialog box

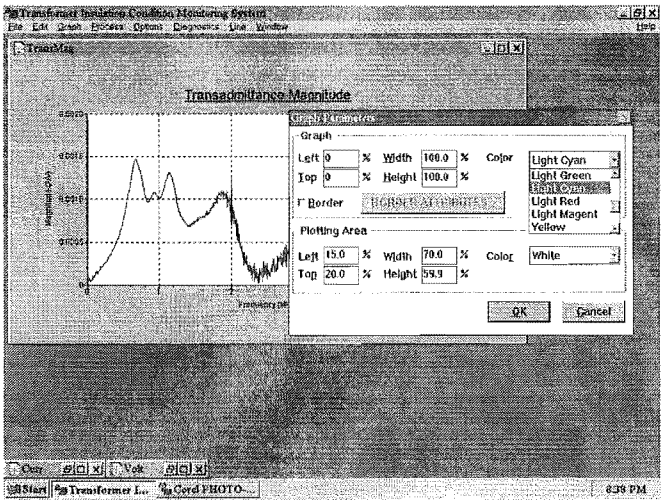


Figure 6.10 Graph parameters dialog box

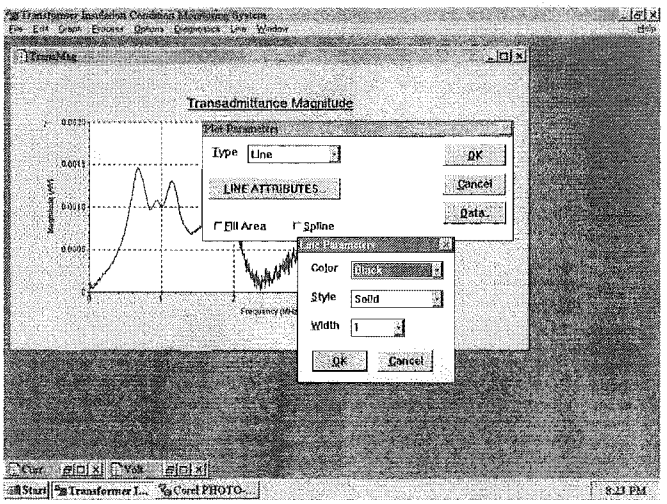


Figure 6.11 Plot parameters dialog box

Selecting the data option in the plot parameters dialog box in Figure 6.11, displays the raw data window as shown in Figure 6.12. The raw data window allows the data to be converted to a desired format and saved to a text file. This option was used during development for getting the data into MATLAB so that various digital signal processing algorithms being trialed could be tested on real data before being committed to DSP code.

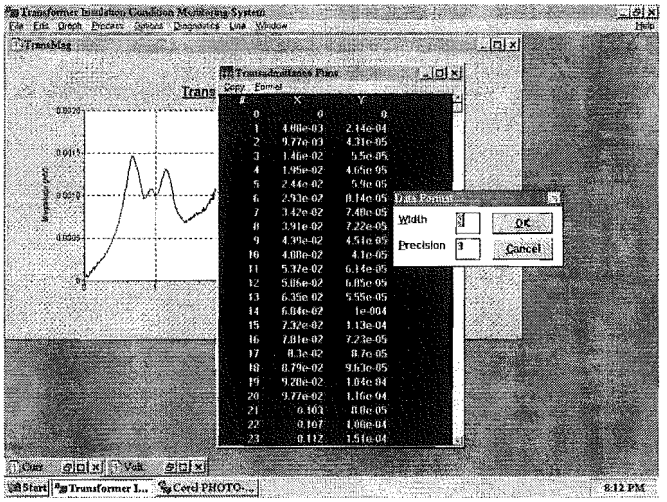


Figure 6.12 Raw data window for transadmittance magnitude data

6.4.1.3 Other Options

Menu options are available that allow the user to save the displayed data to a disk file, and at a later date to open the file and re-display the data. Saved data is time-stamped through the use of the CMOS clock on the PC motherboard. The file open dialog box is illustrated in Figure 6.13. Menu options are also available to select and setup a printer and to print a selected display window as shown in Figure 6.14.

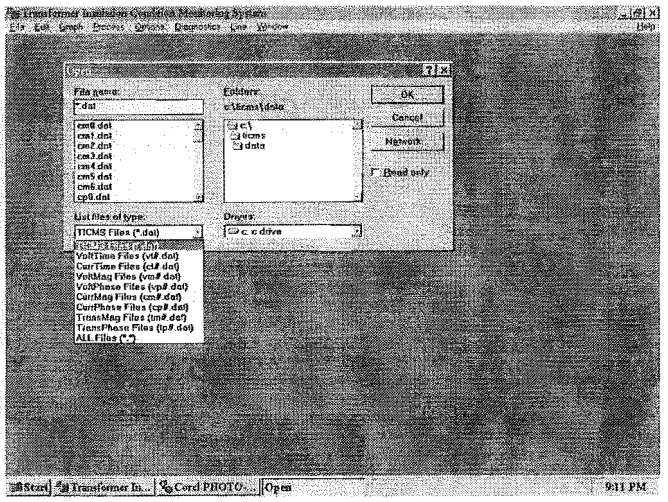


Figure 6.13 Disk file open dialog box

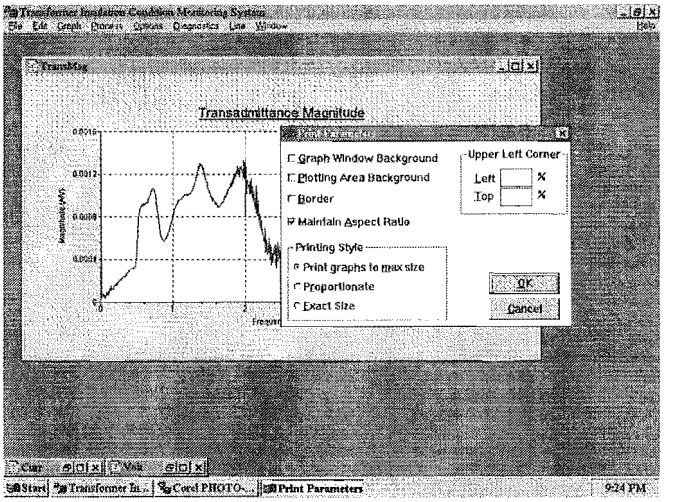


Figure 6.14 TICMS application printing options

A serial port options dialog box is also provided to ensure that the COM port to which the DAPM is cabled is operating in the same mode as the DAPM UART. The serial port options dialog box is illustrated in Figure 6.15.

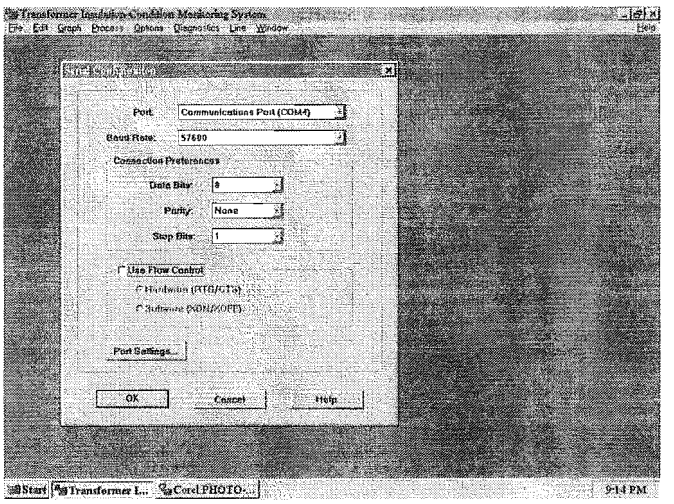


Figure 6.15 Serial port configuration options

6.4.2 Serial I/O Interface

A serial handshake protocol is used to establish a connection between the PC and the DAPM. Because both the PC and the DAPM are configured as DTE devices, a null modem connection is required between the two as shown in Figure 6.16 a). The serial handshake protocol timing is illustrated in Figure 6.16 b). Because there is an inversion between the 16550 register bits and the RTS/CTS outputs pins and another inversion between the output pins and the RS-232 lines (due to RS-232 line drivers), the RS-232 voltage levels shown in Figure 6.16 b) are equivalent to the software logic polarities.

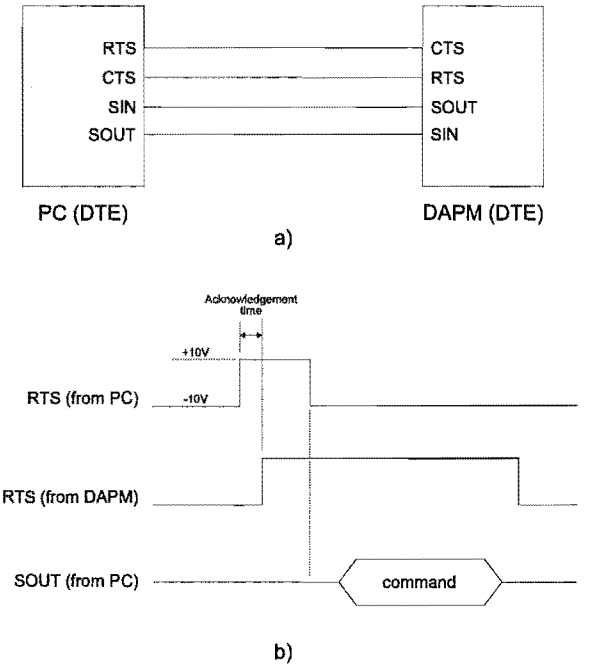


Figure 6.16 a) PC-DAPM serial connection b) Serial handshake protocol

To establish a connection the PC drives it's RTS output line high. In response the DAPM drives it's RTS output line (CTS input to PC) high as an acknowledgement to the PC. In response to the acknowledgement the PC drops it's RTS output line (ready for the next command transmission) and transmits the on-line command. After the DAPM receives the on-line command it drops it's RTS output line, ready for the next command transmission. If the acknowledgement time indicated in Figure 6.16 b) exceeds 5s the TICMS application times out. This prevents the system from locking up if the user forgets to connect the DAPM before going on-line.

When all eight data types are requested, the number of data bytes transmitted is equal to

$$2048(\text{samples}) \cdot 5 \cdot 4(\text{bytes / sample}) = 40960 \text{ bytes} \tag{6.2}$$

where 2048 samples are taken on the voltage and current channels respectively, a 2048 point FFT is used, only the positive frequencies are kept for the magnitude and phase of the voltage, current and transadmittance function, and a C31 word is 4 bytes. At the maximum baud rate of 115200bps, the serial transmission time for this data is

$$\frac{40960(\text{bytes}) \cdot 8(\text{bits / byte})}{115200(\text{bits / second})} = 2.84\text{s} \tag{6.3}$$

Sending only the transadmittance function magnitude for positive frequencies (spectra has conjugate symmetry), results in a transmission time of

$$\frac{4 \cdot 1024(\text{bytes}) \cdot 8(\text{bits / byte})}{115200(\text{bits / second})} = 0.28\text{s} \qquad (6.4)$$

Because the digital signal processing operations complete much faster than the serial transmission time, sending just the transadmittance function magnitude allows the display to be updated in real-time.

Of the 128K of DAPM static RAM, only 8K is reserved for program code. The DSP application software uses 10K of RAM for data storage when processing the time domain data for a single test. This leaves 110K available for buffered data storage when the 'capture data before processing and sending' option is selected. If only the transadmittance magnitude is buffered then the results of up to 110 insulation tests can be buffered before being sent to the PC. This is useful when the requested interval between insulation tests is less than the serial transmission in Eq. (6.4). Buffering additional data types per test reduces the number of test results that can be buffered.

6.5 References

[1] Mynatt B.T., **Software Engineering with Student Project Guidance**, Prentice-Hall Inc., 1990

[2] Sommerville, **Get details from library**,

[3] Petzold C., **Programming Windows 95**, Microsoft Press, 1996

[4] Campbell J., **C Programmer's Guide to Serial Communications**, 2nd ed., Sams Publishing, 1994

Chapter 7

RESULTS

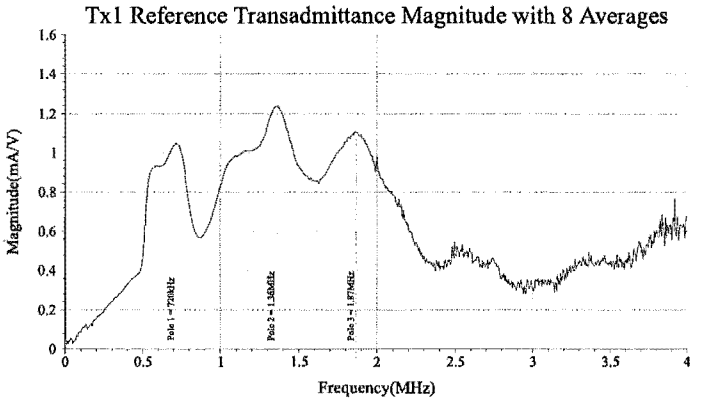
The purpose of this chapter is to present the TICMS results from a series of tests designed to evaluate the effect of known faults and operating conditions on the transadmittance function of a single phase 7.5kVA distribution transformer. The first section presents reference transadmittance functions that are used as a basis for comparison in subsequent sections and describes the characteristics of transadmittance function poles that are monitored for change. Subsequent sections present the results of test sets designed to evaluate the effects of artificial faults, transformer internal temperature changes, and core magnetization on the transadmittance function.

7.1 Reference Measurements

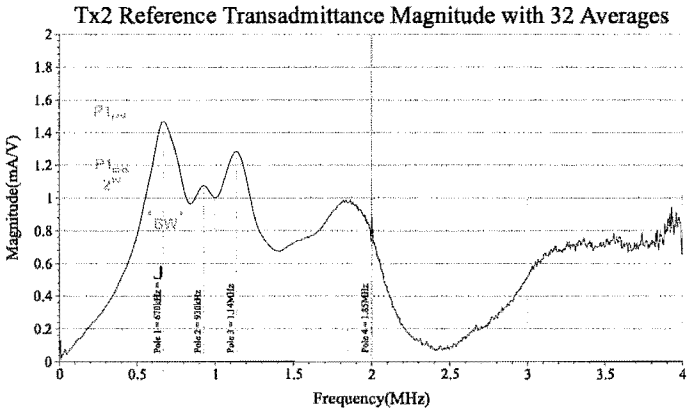
Two single phase 7.5kVA distribution transformers were employed for the test sets conducted in this chapter. The first is referred to as Tx_1 and was used for the temperature and on-line test sequences. The second is referred to as Tx_2 and was used for the artificial fault tests. Tx_2 was not used for the temperature or on-line tests as the integrity of it's winding insulation was compromised by the artificial fault placement procedure. Further, it is dangerous to energise a transformer with shorted winding sections as high current flow results from having an emf induced in a near zero resistance conductor loop.

Prior to conducting tests, the transadmittance functions of Tx_1 and Tx_2 were determined so that they could be used as a basis for comparison. Figure 7.1 presents the reference transadmittance functions. Each was measured with the TICMS operating in averaging mode in order to reduce the amount of noise present at the higher frequencies. Averaging mode is discussed in further detail in 5.7. It can be seen that, Tx_1 has 3 poles at 720kHz, 1.36MHz, and 1.87MHz while Tx_2 has 4 poles at 670kHz, 930kHz, 1.14MHz, and 1.85MHz respectively.

Sweep frequency testing was employed on Tx_1 to verify the transadmittance function



a)



b)

Figure 7.1 a) Tx_1 reference b) Tx_2 reference

determined by the TICMS. The test setup illustrated in Figure 7.2 was used to carry out this procedure. Application of KVL to primary winding loop results in

$$\overline{V}_{trans} = \overline{V}_{in} - \overline{V}_{out} \tag{7.1}$$

By converting Eq. (7.1) to rectangular form and taking the magnitude of the result it is easily shown that

$$|\overline{V}_{trans}| = \sqrt{|\overline{V}_{in}|^2 + |\overline{V}_{out}|^2 - 2|\overline{V}_{in}||\overline{V}_{out}|\cos(\phi_{V_{in}} - \phi_{V_{out}})} \tag{7.2}$$

where ϕ_{Vin} and ϕ_{Vout} are the phase of the input and output sinusoids respectively. Further, the magnitude of the winding current is easily determined as follows

$$|\bar{I}_{trans}| = \frac{|\overline{V}_{out}|}{R_1} \tag{7.3}$$

The magnitude of the transadmittance function is determined at a single frequency by dividing Eq. (7.3) by Eq. (7.2). In summary the sweep frequency testing procedure consists

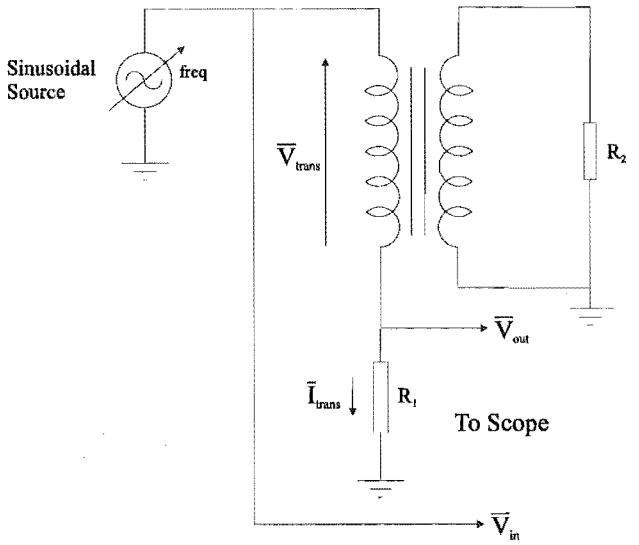


Figure 7.2 Sweep frequency testing setup

of applying a fixed frequency sinusoid, recording $|V_{in}|$, $|V_{out}|$, and $(\phi_{Vin} - \phi_{Vout})$ and then calculating the transadmittance function magnitude at that frequency as detailed above. To determine the transadmittance function over a range of frequencies the source frequency in Figure 7.2 is swept over the band of interest. The transadmittance function of Tx_1 determined using sweep frequency testing is shown in Figure 7.3. It is in excellent agreement with that determined by the TICMS. Differences can be attributed to the accuracy with which the phase difference, $(\phi_{Vin} - \phi_{Vout})$ can be measured.

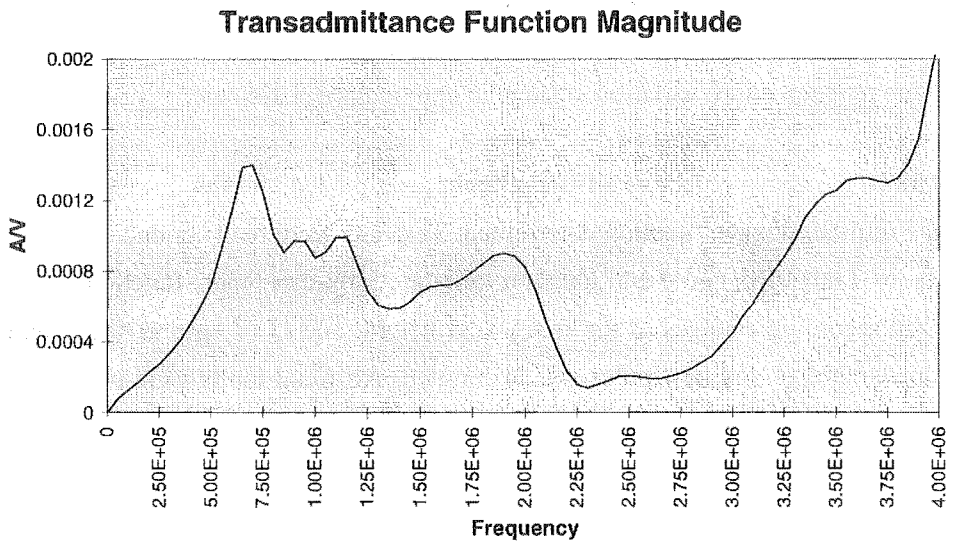


Figure 7.3 Transadmittance function measured using sweep frequency testing

The following pole characteristics were monitored for change during the test sequences presented in this chapter

- **Pole frequency:** The center frequency of the pole
- **Pole height:** The peak magnitude of the pole
- **Pole Q:** The ratio of the pole -3dB bandwidth to its center frequency

These characteristics for the first pole of the Tx_2 reference transadmittance function are illustrated in Figure 7.1 b). Pole Q is a measure of the sharpness of a pole and is defined as follows

$$Q = \frac{BW}{f_{center}} \tag{7.4}$$

where BW and f_{center} are defined in Figure 7.1 b). Percentage changes in the three characteristics were calculated for many of the upcoming results as follows

$$\%\ \text{change} = \frac{(\text{Final value}) - (\text{Initial value})}{\text{Initial value}} \cdot 100\% \tag{7.5}$$

7.2 Effect of Artificial Faults

The effect of different winding insulation faults on the transadmittance function magnitude needs to be determined if the TICMS is to uniquely identify when failure mechanisms are taking place. It is important that the changes brought about are distinguished from those caused by factors discussed in upcoming sections. Failing to do so would mean that the TICMS could incorrectly report a fault, or even worse, miss a fault if the change is thought to be due to temperature variation, change in core magnetization etc.

To achieve the above objective artificial faults were placed into the primary winding of Tx_2 and the transadmittance function determined. Test sets were then conducted to evaluate the effects of fault size and fault location on the transadmittance function. This process involved recording changes in the frequency, height, and Q of each of the original poles. The appearance of any new poles was also noted. Artificial faults were placed to simulate the effects of both local breakdowns and partial discharges. The later were introduced by placing a resistance between two parts of the winding. Separating a local breakdown from a partial discharge is important as the later is tolerable whereas the former is not [5].

The transadmittance function is dependent upon the transformers winding construction. Until suitable models are developed, it is necessary to apply the procedures detailed in this section on a transformer identical to the one that the TICMS is to protect in service.

7.2.1 Transformer Construction

Transformer Tx_2 uses a core-type construction with the primary winding wound over the top of the secondary. Further, both the primary and secondary windings are divided into two coils that are wound on opposite sides of a square core and connected in series as illustrated in Figure 7.4.

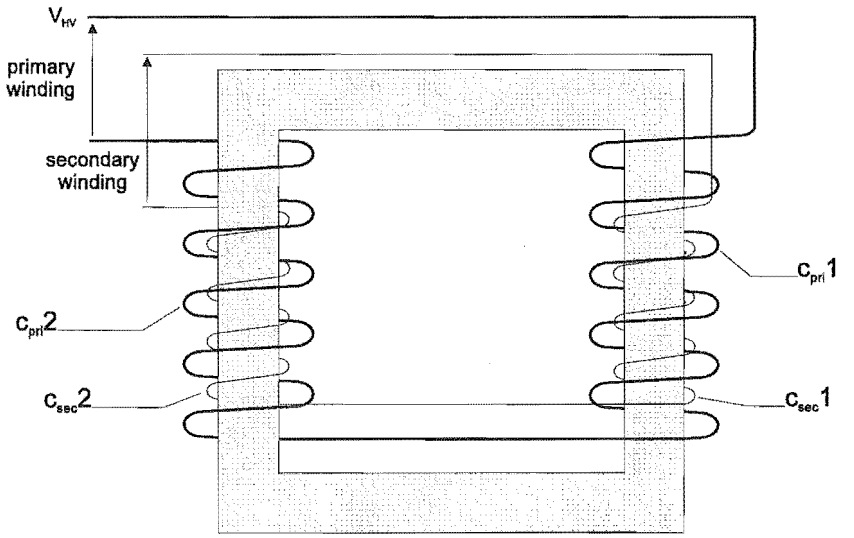


Figure 7.4 Coil winding arrangement of Tx_2

A layer winding consisting of alternate layers of copper winding and paper is used for the primary winding coils, $c_{pri}1$ and $c_{pri}2$. The layered winding arrangement for the beginning of $c_{pri}1$ is shown in Figure 7.5.

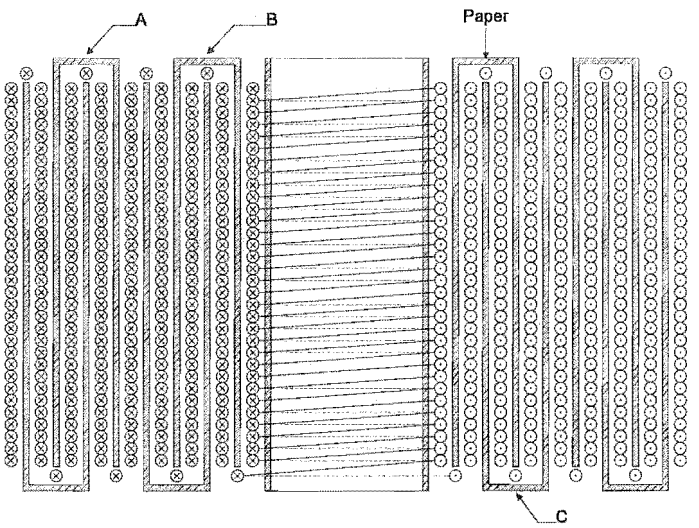


Figure 7.5 Layered winding of $c_{pri}1$

7.2.2 Placement of Artificial Faults

Artificial faults were introduced into the primary winding of Tx_2 by tapping off $c_{pri}1$ at a number of strategic locations. Tapping was performed by cutting away the paper insulation and stripping back the wire insulation from points such as A, B, and C in Figure 7.5, and soldering a length of transformer winding wire to the exposed winding point. The winding wire from each tap point was then connected to a corresponding node on a labeled panel bolted to the top of the transformer, as shown in Figure 7.6. This arrangement allowed artificial faults to be applied quickly by moving a link between different pairs of nodes on the fault panel. During construction care had to be taken to ensure that adequate spatial separation existed between winding wire from different tap points so that the transformer winding insulation integrity was not compromised. Appendix G contains photographs taken during the disassembly and fault construction process.

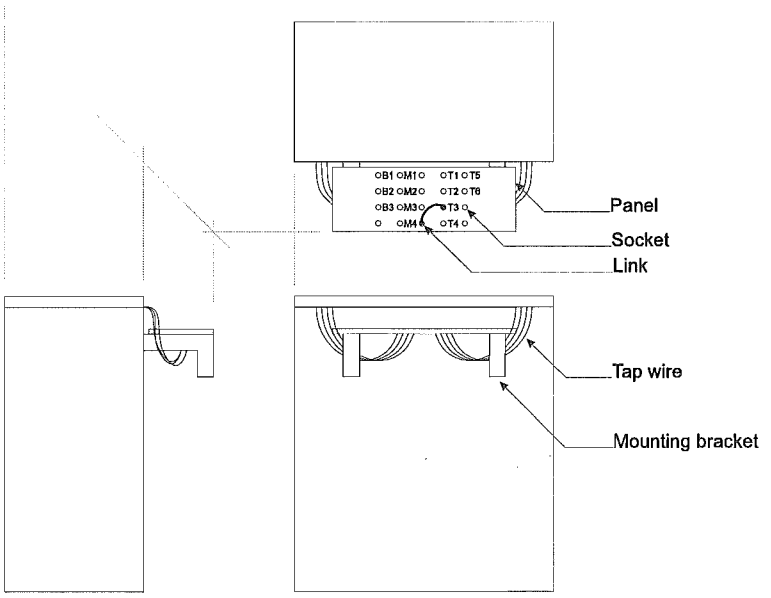


Figure 7.6 Placement of faults into winding of Tx_2

The panel labeling convention in Figure 7.6 uses T, M, and B to indicate taps points that have been taken from the top, middle, and bottom of $c_{pri}1$ respectively. The placement of each tap point along with the number of layers of paper insulation between the taps points is illustrated in Figure 7.7. The number of copper layers is calculated from the number paper layers as follows

$$C_{layers} = P_{layers} + (P_{layers} + 1) \tag{7.6}$$

where C_{layers} and P_{layers} represent the number of copper layers and paper layers respectively.

Eq. (7.6) is readily verified with reference to Figure 7.8, showing the number of copper

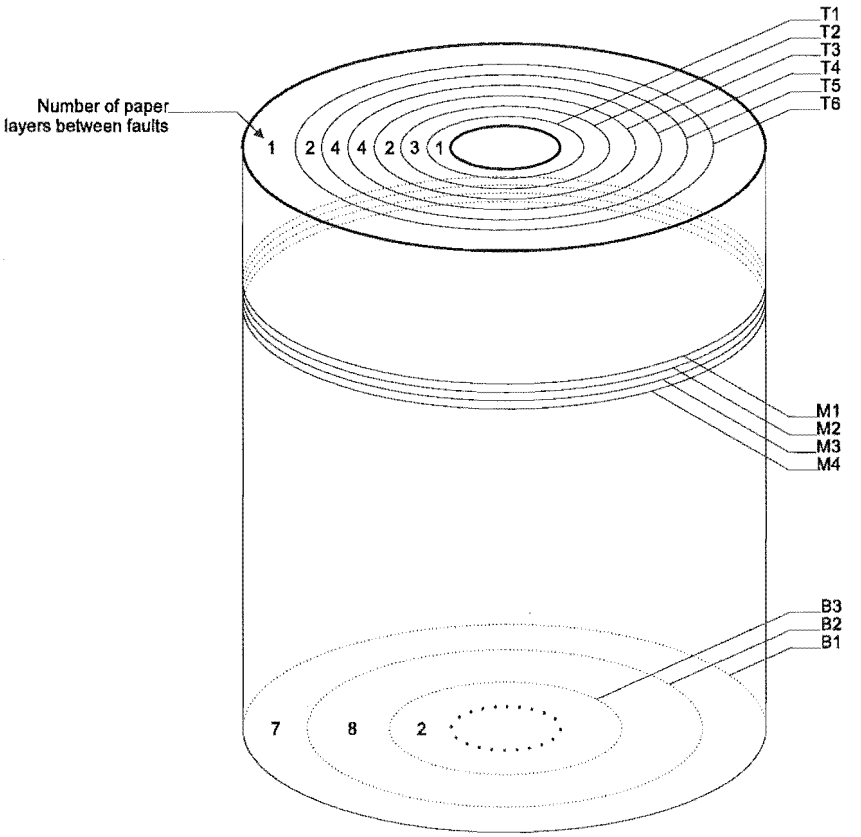


Figure 7.7 Placement of taps for introduction of artificial faults

layers between two example taps points.

From Figure 7.7, the total number of paper layers for $c_{pri}1$ is 17. It follows from Eq. (7.6) that the total number of layers of copper is equal to 35. Further, the number of turns on the outer layer is equal to 205, allowing the total number of turns for the primary winding to be calculated as follows

$$205(\text{turns / layer}) \cdot 35(\text{layers / coil}) \cdot 2(\text{coils / winding}) = 14350(\text{turns / winding}) \quad (7.7)$$

The proximity of each tap point to the HV end of coil $c_{pri}1$ can be determined by measuring the DC resistance between the two points. These resistances have been measured using a Wheatstone bridge and are presented in Table 7-1.

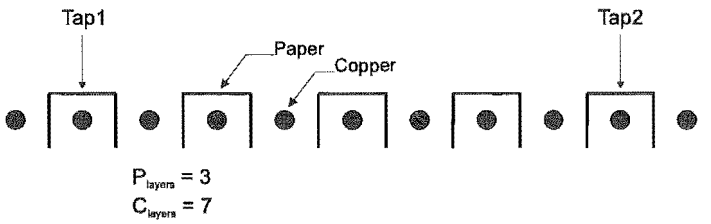


Figure 7.8 Copper and paper layers

Tap point	Resistance to V_{HV} (Ω)*	Tap point	Resistance to V_{HV} (Ω)
T1	96.8	M4	2.4
T2	84.9	B1	6.6
T3	73.1	B2	42.2
T4	48.5	B3	90.7
T5	22.8	Tap 1**	5.6
T6	13.3	Tap 2	11.1
M1	2.3	Tap 3	193.1
M2	2.3	Tap 4	198.6
M3	2.4	Tap 5	204.3

* Total winding resistance is 204.4Ω, ** Tap points placed in by manufacturer

Table 7-1 DC resistance from tap point to HV terminal of $c_{pri}1$

7.2.3 *Effect of Fault Size*

The effect of fault size on the transadmittance function was evaluated by applying a link between tap point T6 and each of T5, T4, T3, T2, and T1 in turn. For each fault the following number of copper winding layers are shorted

- **T6-T5 fault:** 5 layers
- **T6-T4 fault:** 13 layers
- **T6-T3 fault:** 21 layers

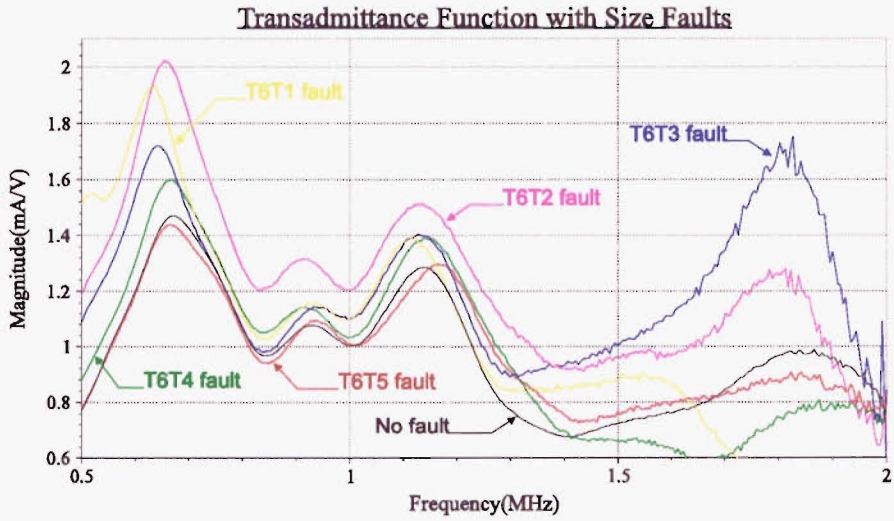


Figure 7.9 Effect of fault size of transadmittance function magnitude

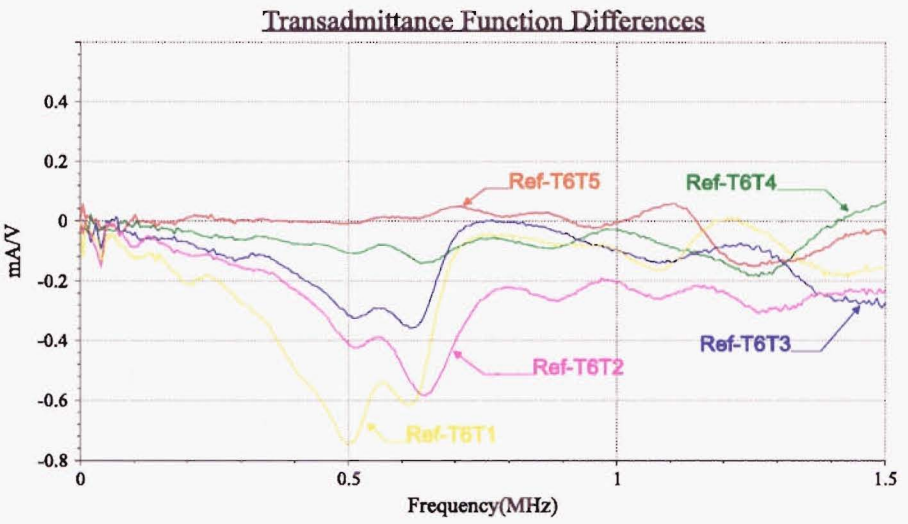


Figure 7.10 Differences between reference and fault transadmittance functions

- **T6-T2 fault:** 25 layers
- **T6-T1 fault:** 31 layers

Figure 7.9 compares the transadmittance functions over the region of maximum change for each of the above faults. Evident is that the height of each of the 4 poles is dramatically

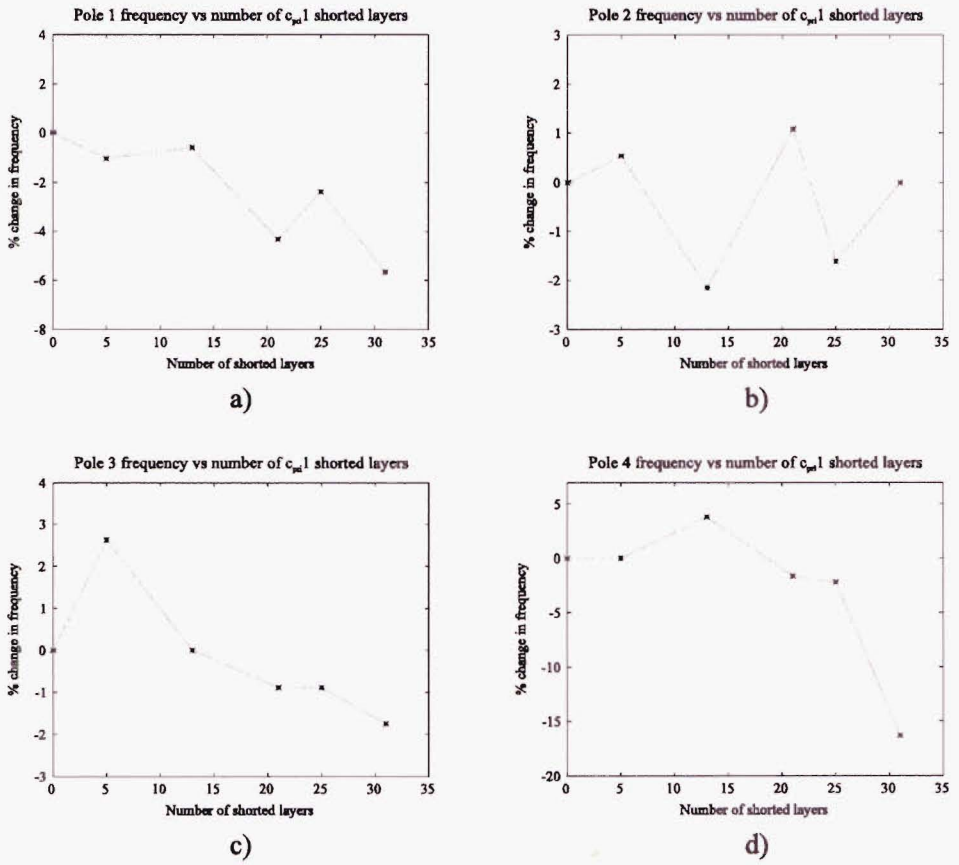


Figure 7.11 Effect of fault size on transadmittance function pole frequencies

effected by shorting out layers of copper winding. To a lesser extent the center frequency of each pole is also effected. The difference between the reference and fault transadmittance functions for each fault is presented in Figure 7.10. Between 0 and 500kHz the difference increases almost linearly with a slope that is proportional to the number of copper layers that are shorted within the winding.

The relationship between the center frequency and the number of shorted copper layers is illustrated in Figure 7.11 for the 4 poles. In general poles 1, 3, and 4 decrease in frequency. Pole 3 decreases almost linearly when the number of shorted layers exceeds 13. For poles 1, 2, and 3 the changes are a few percent at most. Changes up to 20% were measured for the center frequency of pole 4.

Figure 7.12 illustrates the effect of fault size on the height of each pole. In general poles 1, 2, and 3 increase in height almost linearly with the number of shorted layers. Figure 7.13 shows how the Q of pole 1 varies with the number of shorted layers. Little change is seen until 25 layers are shorted. The amplitude of the other poles was insufficient to determine their Q.

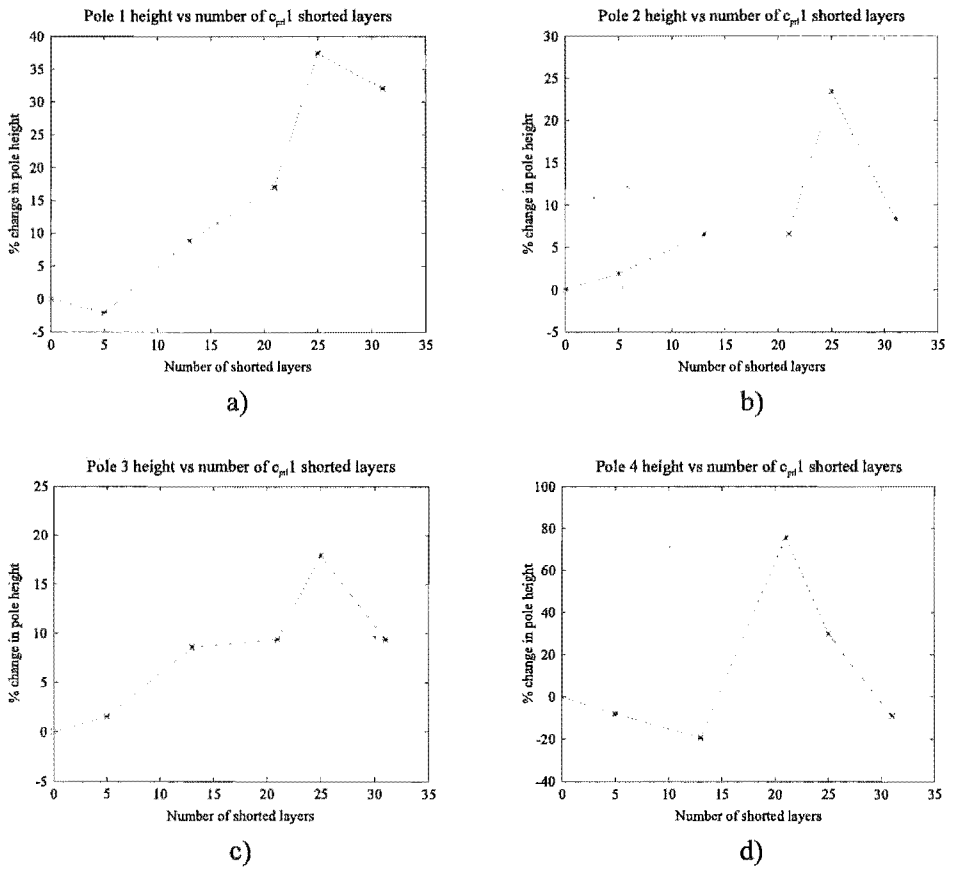


Figure 7.12 Effect of fault size on transadmittance function pole height

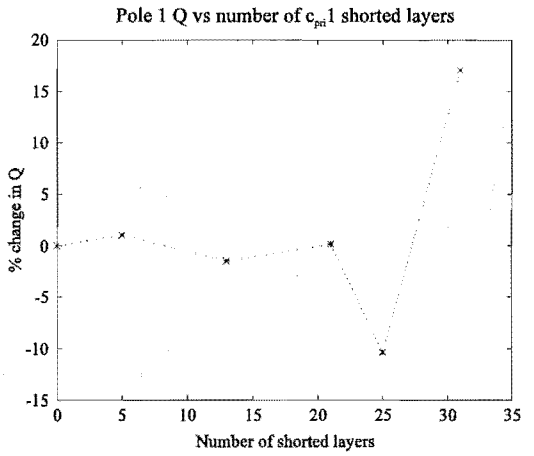


Figure 7.13 Effect of fault size on Q of pole 1

Shorting layers within the winding has an effect on the resonant frequencies within the winding, which shows up as changes in the height and frequency of the transadmittance function poles. The percentage changes in Figure 7.11 and Figure 7.12 show that layer shorts have a greater effect on pole height than on center frequency. The near linear increase in height for poles 1, 2, and 3 indicates that changes occur in the transadmittance function at a lower frequency as the fault size is increased.

The effect of fault size on the characteristics of the poles is of more interest over the first 2 or 3 data points in Figure 7.11 to Figure 7.13, as layer faults experienced by a transformer in service are more likely to be across a smaller number of layers. Further, the results for pole 4 may not be as accurate as those of the lower frequency poles as the fault placement process introduces conductive loops that are potentially a source of error at high frequencies.

7.2.4 Effect of Fault Location

The effect of fault location on the transadmittance function was evaluated by applying a link between tap points T6 and T5, T5 and T4, T4 and T3, T3 and T2, and T2 and T1. The starting layers within $c_{pri}1$ for each fault along with the number of layers shorted are as follows

- **T6-T5 fault:** 3rd layer, 5 layers
- **T5-T4 fault:** 7th layer, 9 layers
- **T4-T3 fault:** 15th layer, 9 layers
- **T3-T2 fault:** 23rd layer, 5 layers

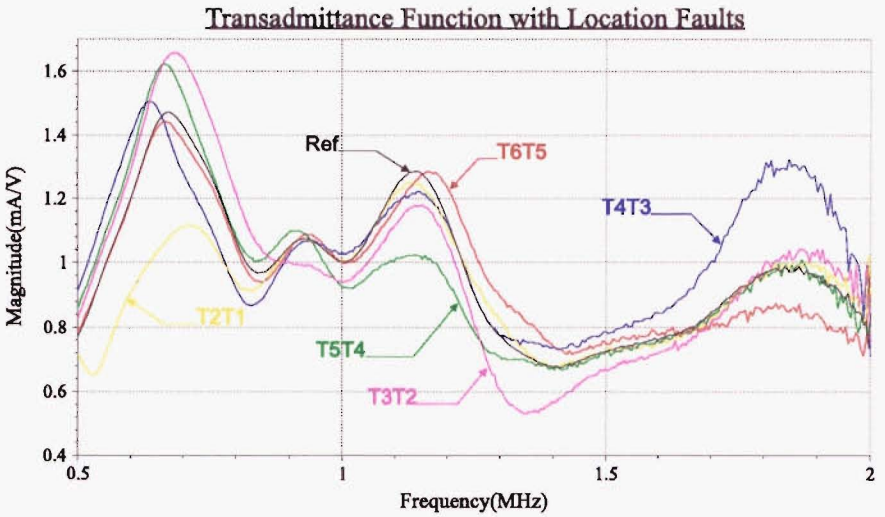


Figure 7.14 Effect of fault location on transadmittance function magnitude

- **T2-T1 fault:** 27th layer, 7 layers

where layer 1 is the outer copper winding layer of $c_{pri}1$. Because the primary winding consists of 2 coils as shown in Figure 7.4, the location faults extend between the HV end and center of the primary winding. Due to the difficulty of accurately placing the tap points, the number of shorted layers for each of the location faults above is not constant. As a consequence fault size differences may have a small effect on the fault location results. However this influence will be limited as the range over which the number of shorted layers varies, is small compared to the total number of layers within $c_{pri}1$.

Figure 7.14 compares the transadmittance functions over the region of maximum change for each of the above fault conditions. Both the center frequency and height of each pole is

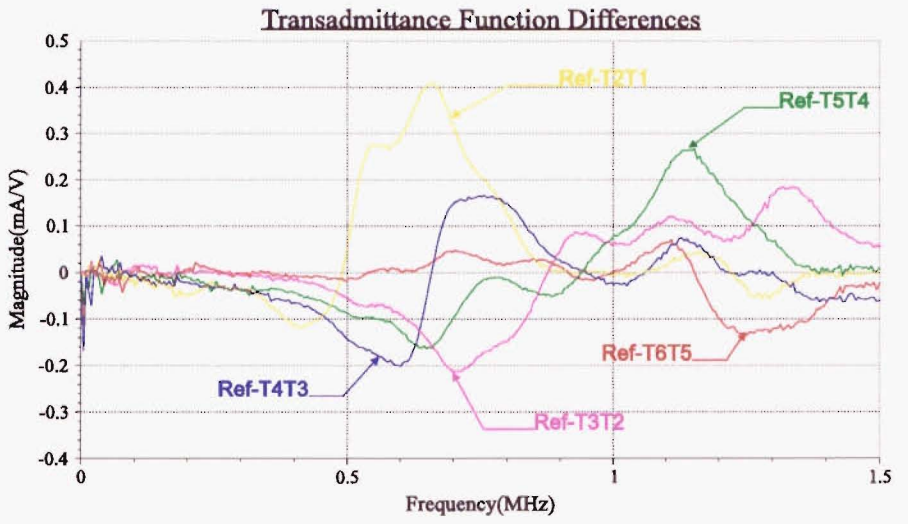


Figure 7.15 Differences between reference and fault transadmittance functions

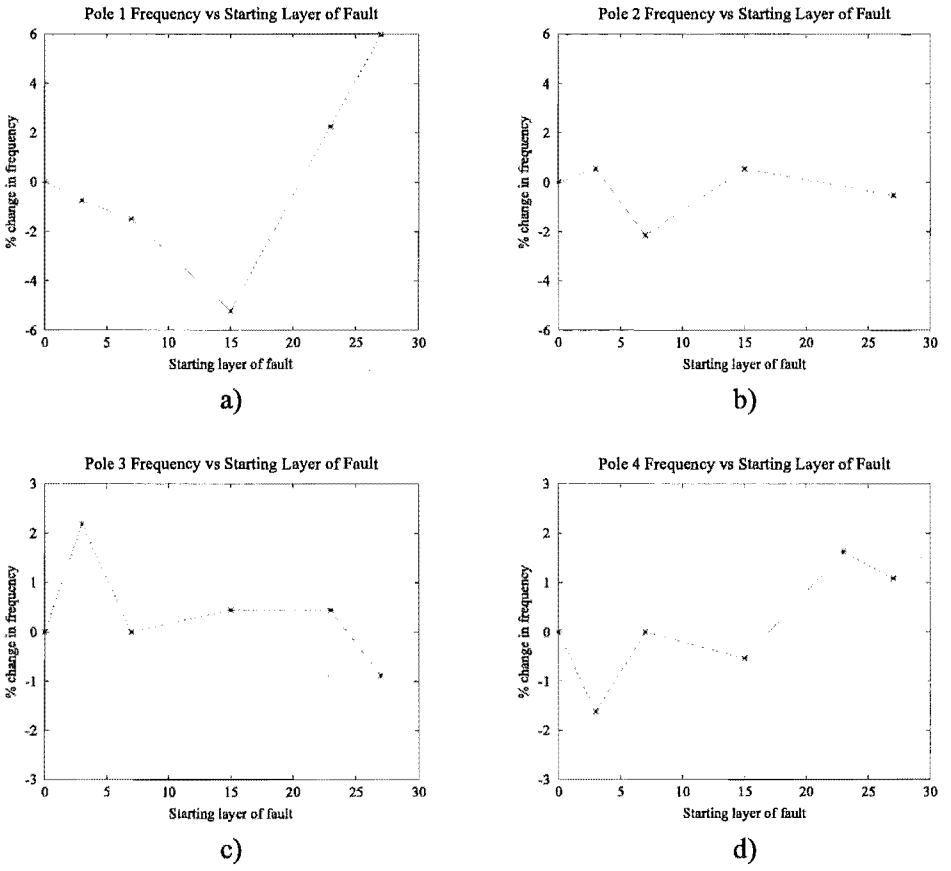


Figure 7.16 Effect of fault location of transadmittance function pole frequencies

effected by the position of the fault. The difference between the reference and fault transadmittance functions for each fault is presented in Figure 7.15. Because the number of shorted layers is relatively small compared to the size faults, little difference is seen between the reference and location fault transadmittance functions between 0 and 500kHz. The frequency at which the peak difference occurs in Figure 7.15 changes with fault location.

The relationship between pole center frequency and fault starting layer is illustrated in Figure 7.16 for the 4 poles. The center frequency of pole 1 reduces to a minimum and then increases as the fault moves towards the middle of $c_{pri}1$. For poles 2, 3, and 4 the centre frequency changes are a few percent at most.

Figure 7.17 illustrates the effect of fault location on the height of each pole. Larger changes were observed for poles 1 and 4. Figure 7.18 shows how the Q of pole 1 varies with the location of the fault. The amplitude of the other poles was insufficient to determine their Q.

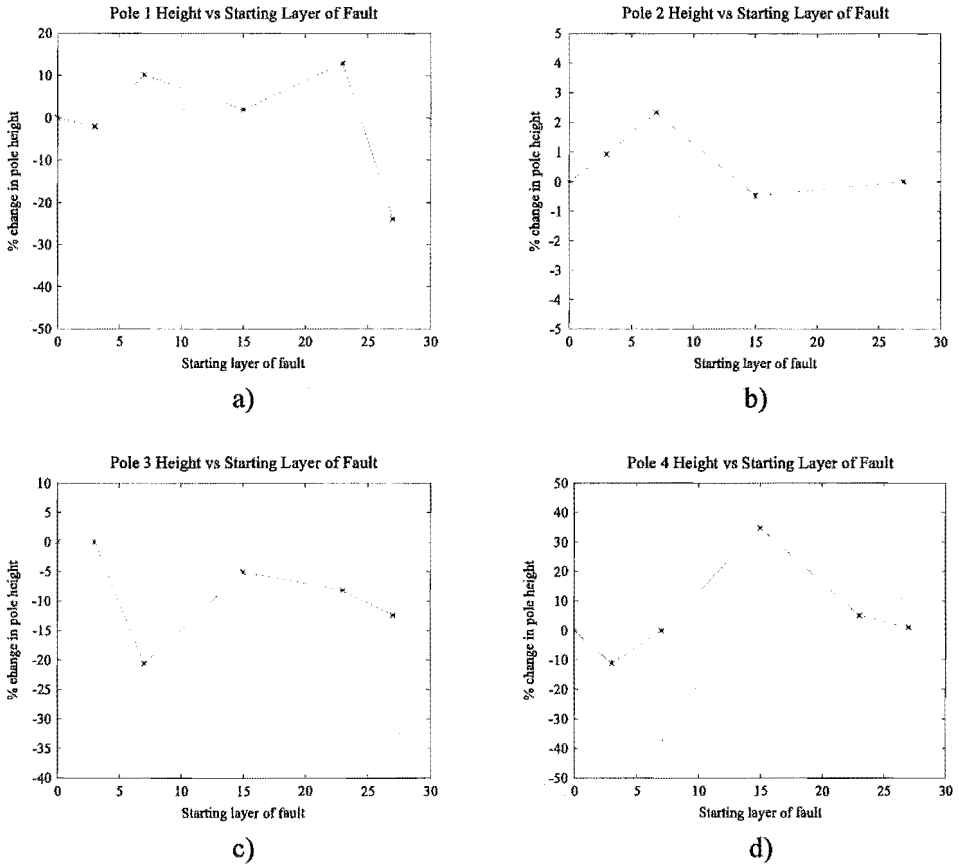


Figure 7.17 Effect of fault location of transadmittance function pole height

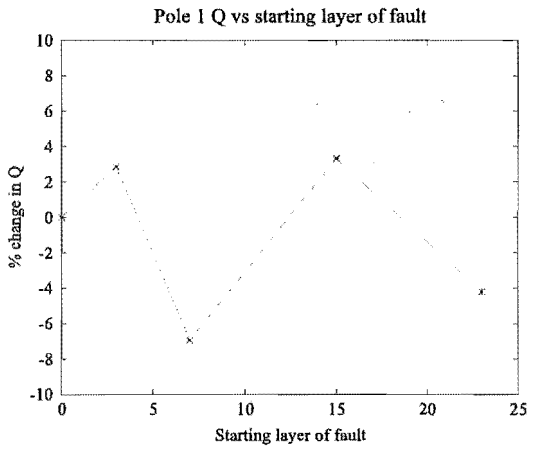


Figure 7.18 Effect of fault location on Q of pole 1

7.2.5 Effect of Simulated Partial Discharge

Simulated partial discharges were introduced by placing a 100Ω resistance between 2 points within the winding. Figure 7.19 show the effect of inserting 100Ω between points T6 and T5, T5 and T4, T4 and T3, T3 and T2, and T2 and T1. Pole height is affected by the introduction of a simulated partial discharge, while center frequency remains essentially

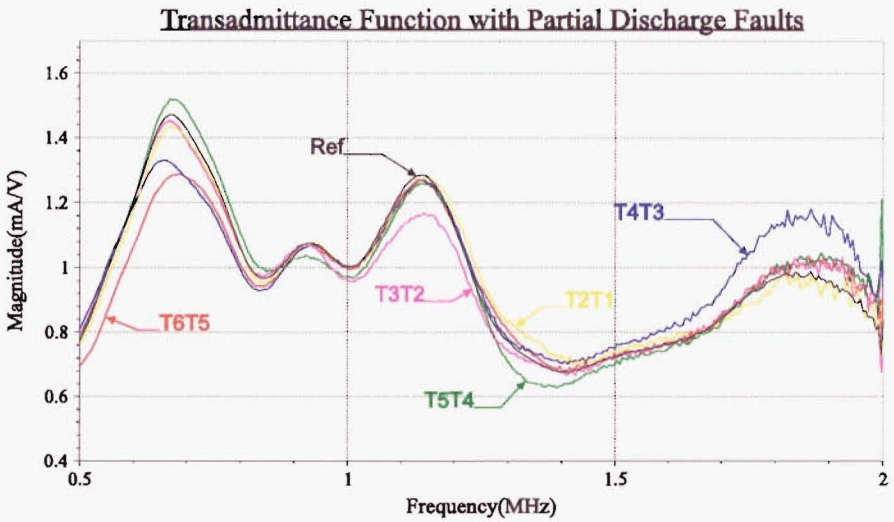


Figure 7.19 Effect of partial discharge faults on transadmittance function magnitude

constant. Figure 7.20 shows the difference between the reference and simulated partial discharge transadmittance functions. Comparing Figure 7.19 with Figure 7.14 reveals that replacing a short with a 100Ω resistance has the effect of reducing the change in pole height. The transadmittance function differences in Figure 7.20 are an attenuated version of those in Figure 7.15.

The observed relationship between pole center frequency and fault starting layer is illustrated in Figure 7.21 for the 4 poles. Figure 7.22 illustrates the effect of PD fault location on pole height. The observed percentage changes are very similar to those obtained for the fault location test. Replacing the short with a 100Ω resistance has reduced the percentage change by half. Figure 7.23 shows how the Q of pole 1 varies with PD fault location. Replacing the short with a 100Ω resistance results in much larger changes to the Q

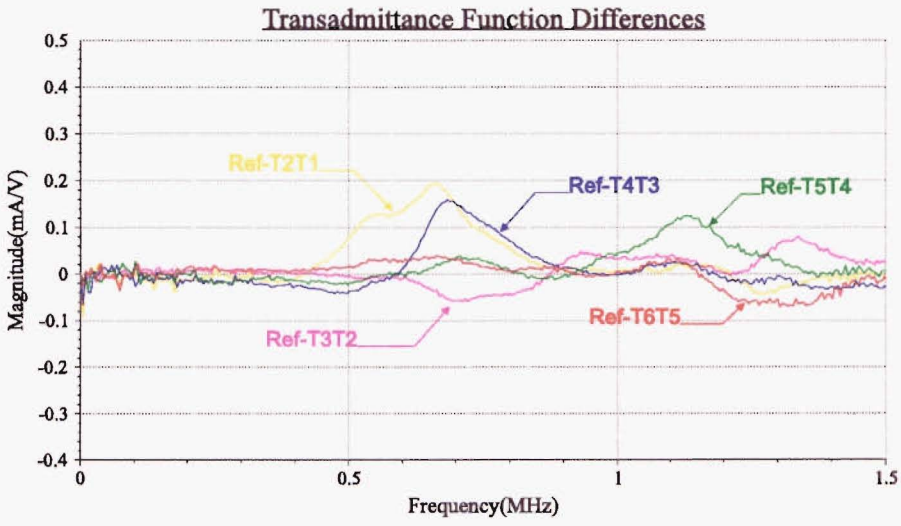


Figure 7.20 Differences between reference and fault transadmittance functions

of pole 1.

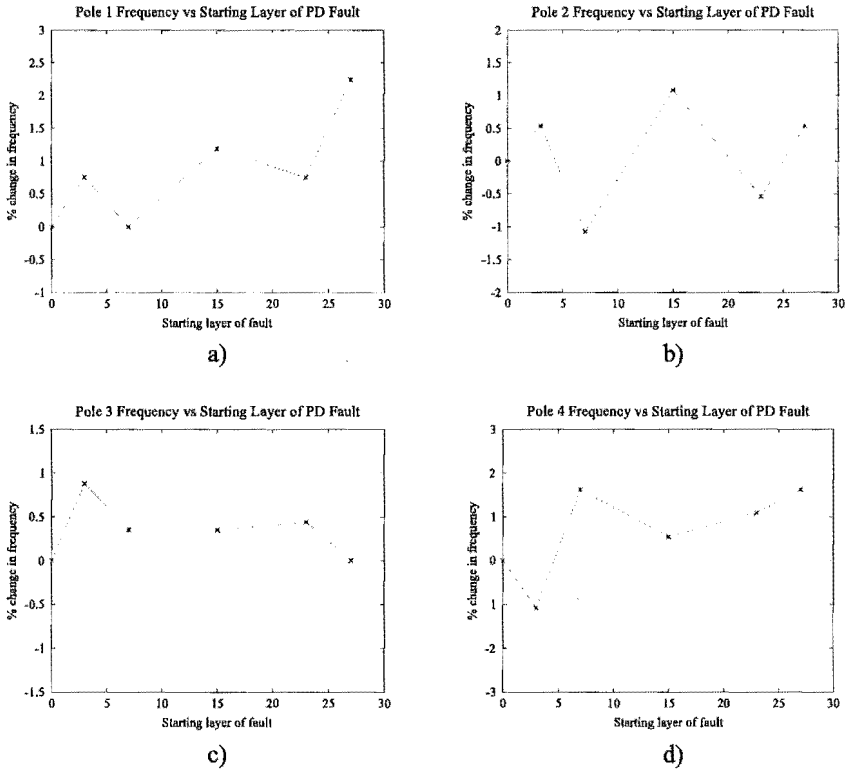


Figure 7.21 Effect of PD fault location of transadmittance function pole frequencies

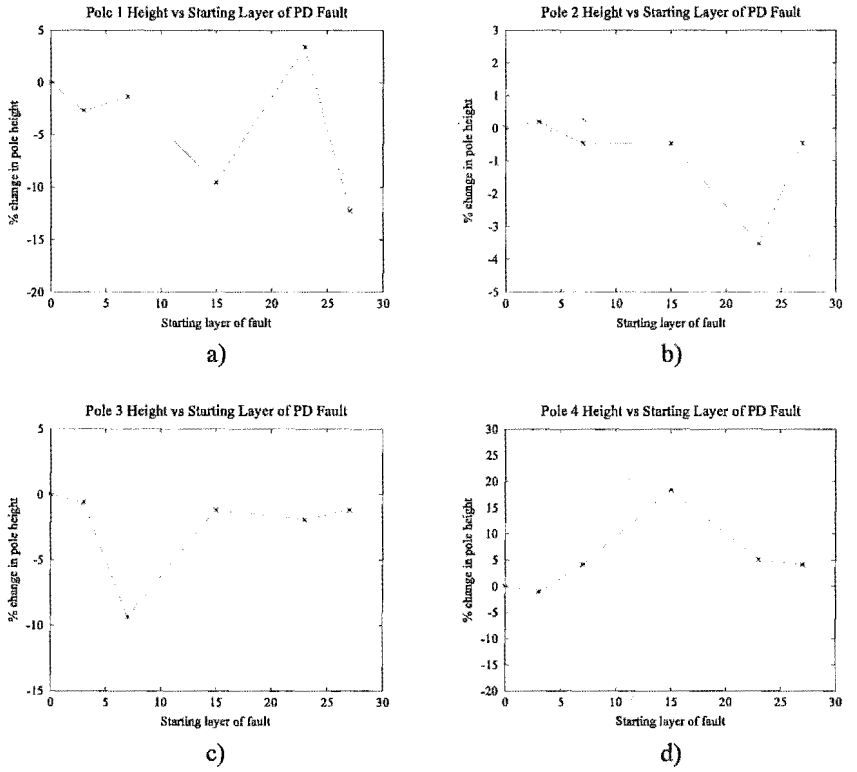


Figure 7.22 Effect of PD fault location of transadmittance function pole height

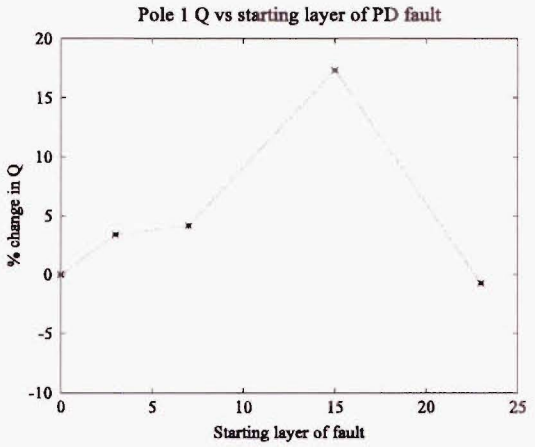


Figure 7.23 Effect of PD fault location on Q of pole 1

7.2.6 Effect of Inter-Turn Faults

The effect of inter-turn faults on the transadmittance function was investigated by applying a link between tap points M1 and M2, M1 and M3, and M1 and M4. These faults short 1, 2, and 3 turns on the outer layer of $c_{pri}1$ respectively. Each fault is located approximately a third of the way down $c_{pri}1$ as shown in Figure 7.7. These single turn faults can also be seen in the color photos presented in Appendix G.

The effect of shorting turns on the outer layer of $c_{pri}1$ is illustrated in Figure 7.24, where the amplitude of pole 3 is increased as the number of shorted turns increases. The fact that 1 turn out of 14350 can have an effect on pole amplitude highlights the sensitivity of the transadmittance function method. Detecting single turn faults is important as they can become catastrophic within a few minutes.

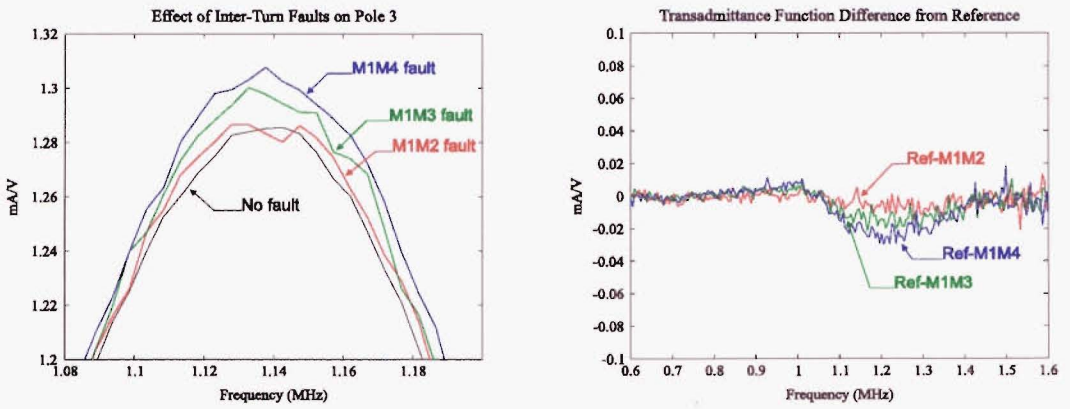


Figure 7.24 Effect of faults between individual turns on pole 3

7.3 Effect of Temperature

A transformer's operating temperature changes as the load it supplies varies with time. As a consequence it is important to know if changes in the transformer's operating temperature have an effect on it's transadmittance function. If so, then the TICMS must be able to distinguish these changes from those caused by internal fault conditions. Failing to do so could cause the system to incorrectly report a fault when load conditions change.

To evaluate the effect of a transformer's internal temperature, the TICMS was used to determine the transadmittance function of Tx_1 at different temperatures. A thermocouple was used to measure the temperature by placing it's wire into the oil via an opening near the top of the tank. Off-line tests were performed at 12°C, 17°C, 32°C, 44°C, and 65°C. The internal temperature of Tx_1 was increased by:

- Supplying the LV winding with 1kVA from a 50A source
- Applying external heat by placing a resistive heating element underneath the tank
- Applying external heat by using a gas torch on the tank walls

7.3.1 Supply Considerations

Because only a low voltage, high current supply (up to 400A rms) was available in the High Voltage Lab, it was decided to supply the LV winding with 50A with the HV winding shorted. Shorting the HV winding increased the current flowing through the transformer thus maximising the copper loses (I^2R loses), which are a dominant source of heat in a transformer. Under these conditions 1kVA was drawn from the supply. Because Tx_1 is rated at 7.5kVA, the 1kVA being supplied had a limited heating effect. The supply current could not be increased further, as this would exceed the current rating of the LV winding.

The efficiency of a transformer is defined as follows:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{copper} + P_{core}} \tag{7.8}$$

When more power flows into a transformer, more power will be dissipated within the transformer. Core losses increase as the supply voltage increases while copper loses increase as more current is drawn. Loading the HV winding to increase the power flow through the transformer was not possible as the resistive loads available could not handle the required power dissipation. Adding a reactive load would be of no use as an increase in real power dissipation is needed to heat the transformer. As a result the external heat sources previously mentioned were needed to heat the transformer to a sufficient

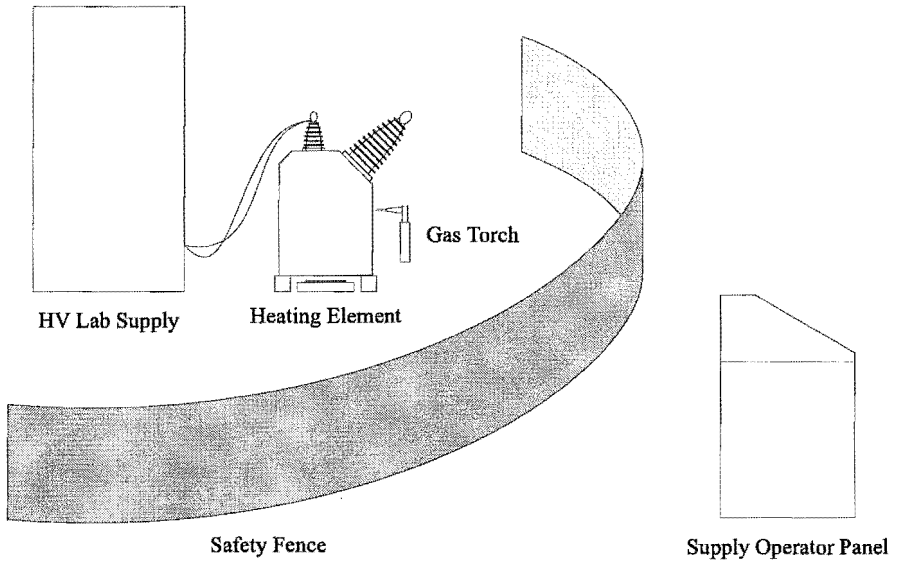


Figure 7.25 High Voltage Lab test setup

temperature. The equipment arrangement used is illustrated in Figure 7.25.

7.3.2 Experimental Procedure and Results

Testing was performed over a period of two days. On day one a reference transadmittance function was determined before applying any heat. The internal temperature was 17°C when the reference was determined. The reference shown in Figure 7.26 has major poles at 720kHz, 1.36MHz, and 1.87MHz which are referred to throughout this section as pole 1, pole 2, and pole 3 respectively. The transadmittance function was next determined on the morning of day two, after a heavy overnight frost. For this test the internal temperature was 12°C. The three sources of heat were then applied for about 30mins to bring the internal temperature up 32°C. The LV winding supply was then disconnected, the external heat

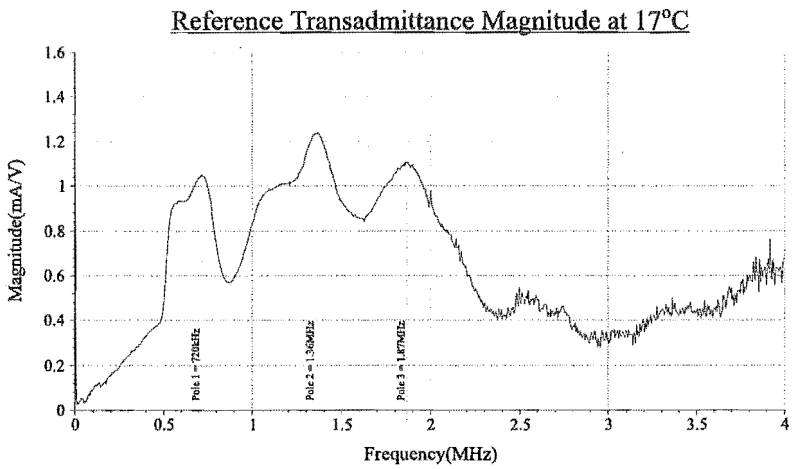


Figure 7.26 Reference transadmittance function of Tx_1

sources turned off, the resistive element removed from under the tank, a load added to the LV winding and the TICMS connected. The transadmittance function was then determined using 8 averages. The internal temperature dropped by 1°C during the period of time over which no heat was applied. The small drop can be attributed to the large thermal mass of the transformer.

The procedure was then repeated to determine the transadmittance function at 44°C and 65°C. Heat was applied for about 30 and 60 minutes to bring the temperature up to 44°C and 65°C respectively. Temperature drops of 1°C and 1.5°C occurred at 44°C and 65°C respectively during the tests. To limit the drop at 65°C the resistive element was left under the tank after it had been turned off. The element was turned off to prevent the element current magnetic field from affecting the measurements. The transadmittance function determined at each temperature is illustrated in Figure 7.28. The reference transadmittance function is shown shaded in Figure 7.28 for easy comparison.

Figure 7.28 shows that the pole frequency of each pole decreases as the internal temperature increases. This is better illustrated in Figure 7.27, which shows the transadmittance function at each temperature over a frequency range that includes the major poles. Further analysis on the data contained in Figure 7.27 allows more accurate relationships to be developed that describe how pole frequency is affected by increasing internal temperature. The observed relationship is illustrated in Figure 7.29, which shows that pole frequency decreases linearly with respect to temperature and that the rate of decrease for a given pole, increases linearly with respect to the initial pole frequency. Figure 7.29d) showing the rate of change of pole frequency was constructed from the line of best fit in Figure 7.29a) to Figure 7.29c).

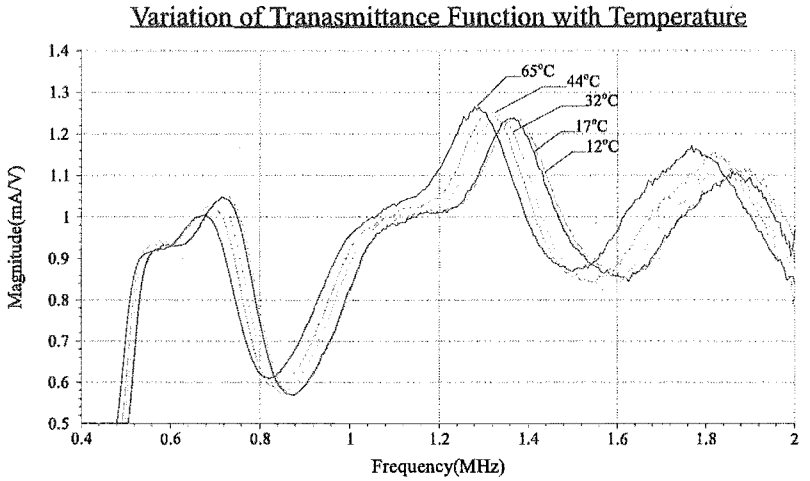


Figure 7.27 Variation of pole characteristics with respect to temperature

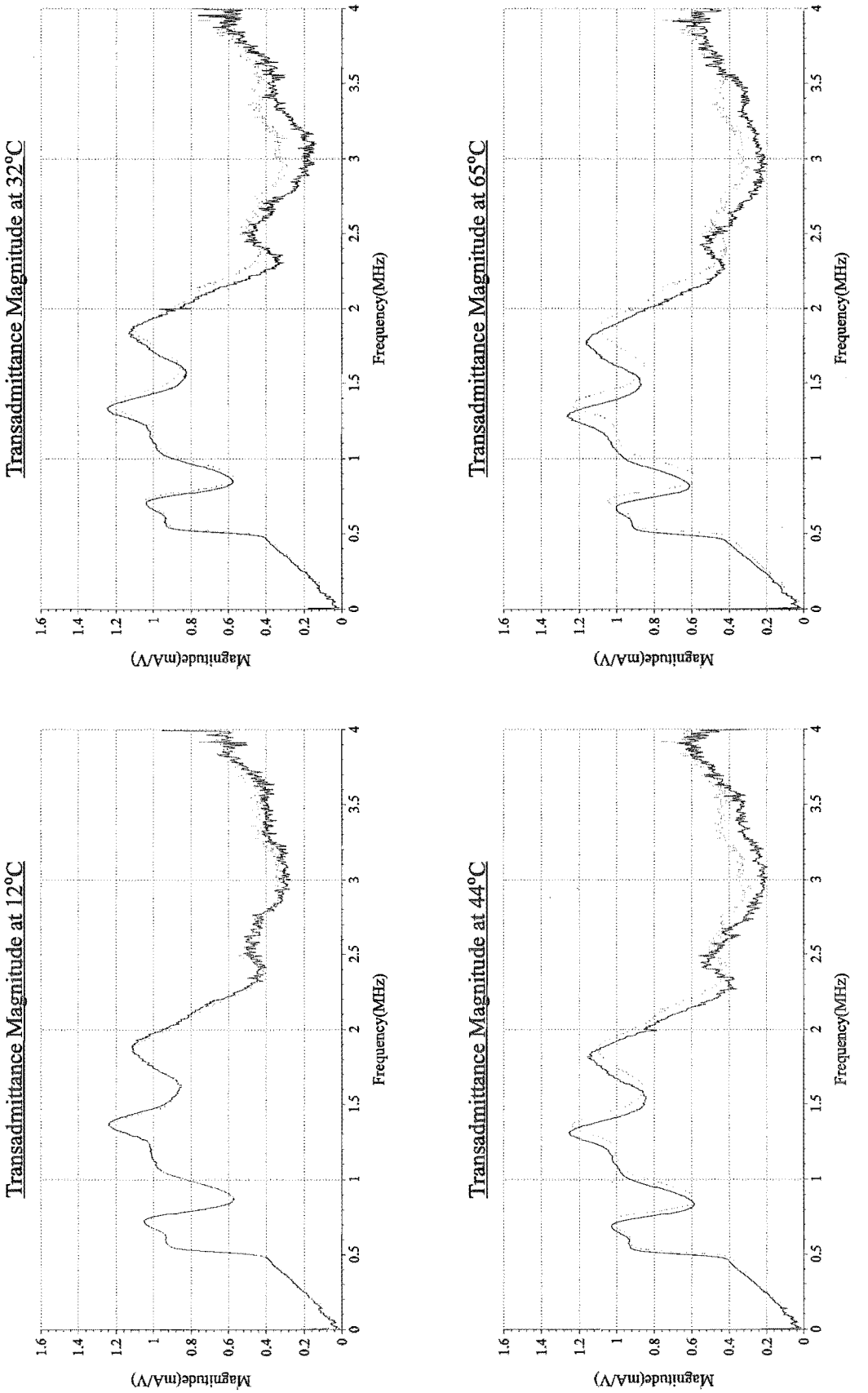


Figure 7.28 Transadmittance function magnitude of Tx_1 at 12°C, 32°C, 44°C and 65°C

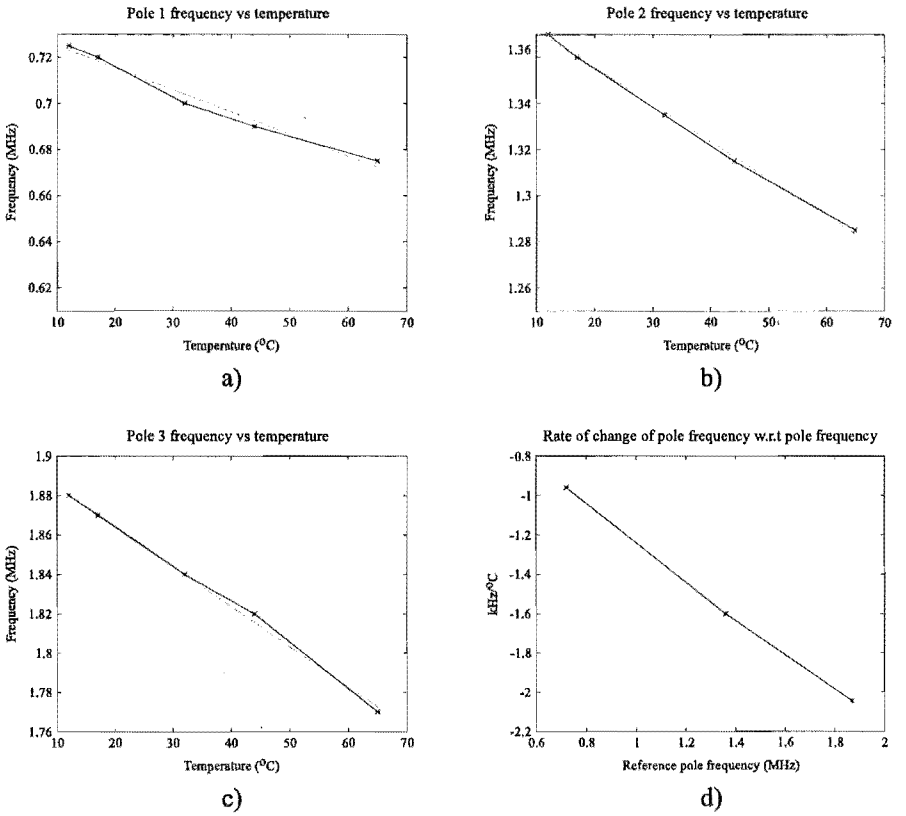


Figure 7.29 Effect of temperature on pole frequency

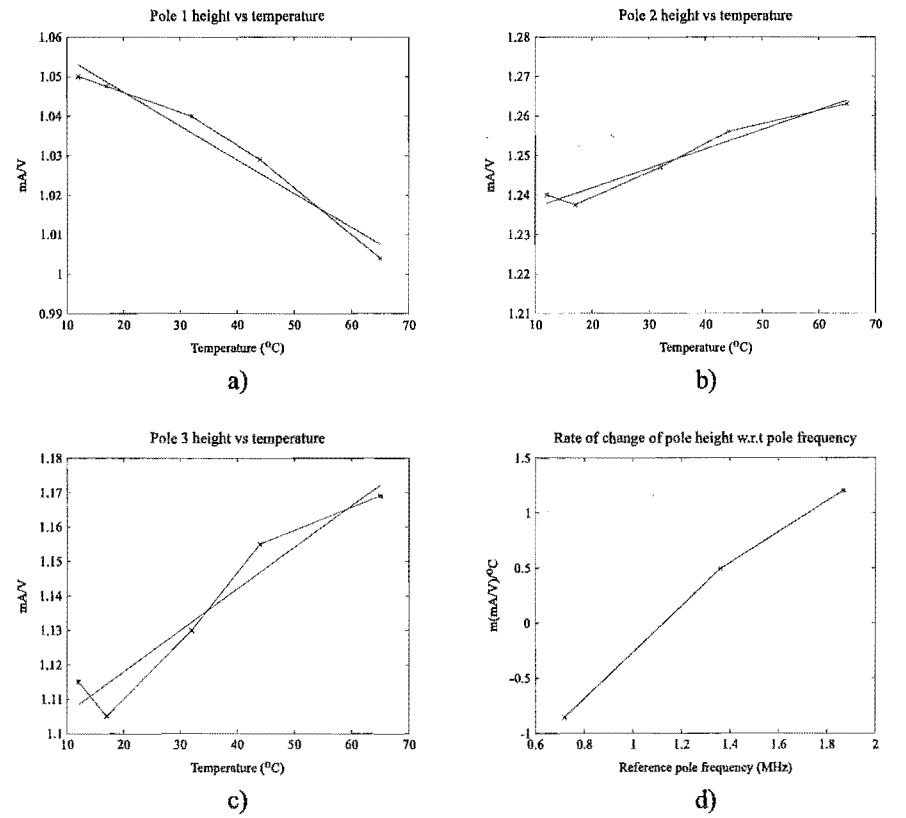


Figure 7.30 Effect of temperature on pole height

Further analysis on Figure 7.27 allows the effect of internal temperature on pole height to be quantified. Figure 7.30 result from this analysis, and shows that in general pole height changes linearly with respect to temperature and that the rate of change of pole height is proportional to the initial pole frequency. Figure 7.30d) was constructed from the line of best fit in Figure 7.30a) to Figure 7.30c).

The linear nature of the pole frequency and height results allow extrapolations to be made to cover transformer operating temperatures exceeding 65°C. As a further implication, linear models along with a temperature input can be incorporated into the TICMS, allowing transadmittance function changes brought about by temperature to be separated from those arising from winding insulation faults.

Throughout the heating process it was noted that the external sources were doing the majority of the heating. As a consequence heat had to penetrate the paper layers to reach the solid insulation of the windings. Typically electrical insulators are also good thermal insulators and as a result some of the externally applied heat may not have reached the interior of the winding in the time interval over which the tests were performed. The oil temperature measured by the thermocouple therefore may not have been the same as that within the winding. For a transformer in service, heat is generated from within the windings and must penetrate the solid insulation layers to reach the oil and tank. Clearly the application of external heat leads to a different temperature distribution within a transformer and as a result the magnitude of the changes illustrated in Figure 7.27 may differ from those experienced by a transformer in service. As a result further temperature testing needs to be done on transformers in service in order to construct more accurate models.

7.4 On-Line Test Results

On-line testing was performed as the TICMS is ultimately aimed at determining the transadmittance function of a transformer while it is in service. Tests were conducted to evaluate how the transadmittance function is affected by

- **The magnitude of the AC supply voltage**: The effect of this needs to be evaluated as the supply voltage of a transformer can depend on the tap changer setting of a driving transformer and other power system parameters. Distinguishing the effect of supply voltage changes on the transadmittance function (if any) from insulation condition deterioration prevents the TICMS from reporting a fault when the power system configuration is altered.

- **The magnitude of the load current drawn from the transformer**: The effect of this needs to be evaluated due to the dynamic variation of transformer load currents. Differentiating the effect of load current variations on the transadmittance function (if any) from insulation condition deterioration prevents the TICMS from reporting a fault when power system loads change during peak demand periods.
- **The point in the 50Hz cycle when the test is performed**: The magnetisation of the iron core of a transformer varies on a cyclic basis throughout the 50Hz cycle. To determine if the core magnetisation has a measurable effect on the transadmittance function, tests synchronised to the 50Hz cycle were conducted.

Figure 7.31 shows the basic setup used for performing on-line tests. Color photos of the equipment setup are given in Appendix I. The additional peripheral equipment shown has no effect on the transadmittance function as the DAPM still digitises the voltage across and the current through the primary winding of the transformer under test. Further, the transformer acts as a low pass filter attenuating the frequency components of interest (above 50Hz to 3MHz). This effectively isolates the measurement system from the transformers load impedance. As shown, the transformer is supplied with an isolated 50Hz supply while the TICMS determines the transadmittance function. A coupling capacitor (C_c) is used to couple the impulse from the IGM onto the HV terminal of the primary winding. Because the 50Hz reactance of C_c is equal to

$$X_C = \frac{1}{2\pi \cdot 50 \cdot 10 \cdot 10^{-9}} = 318.3\text{k}\Omega \tag{7.9}$$

then a maximum voltage of

$$\frac{240 \cdot [(330+47)//(1/2\pi \cdot 50 \cdot 10 \cdot 10^{-9})]}{318.3\text{k} + [(330+47)//(1/2\pi \cdot 50 \cdot 10 \cdot 10^{-9})]} = 0.28\text{V} \tag{7.10}$$

is setup on C_2 of the IGM (see Figure 4.2) by the supply voltage to the transformer under test. Further, both C_c and C in Figure 7.31 need a voltage rating capable of withstanding a peak voltage 340V. This voltage occurs when the transformer is supplied with full voltage. In a power system the voltage rating of C_c and C would need to be much higher due to the increased amplitude of the supply voltage.

As discussed in 4.4.1, the RC high pass filter on the voltage channel in Figure 7.31 prevents the large amplitude 50Hz component from taking up any of the dynamic range of the voltage channel of the DAPM. Further, 4.4.1 shows that the RC filter provides 90dB of attenuation at 50Hz. A supply voltage of 220kV would therefore present

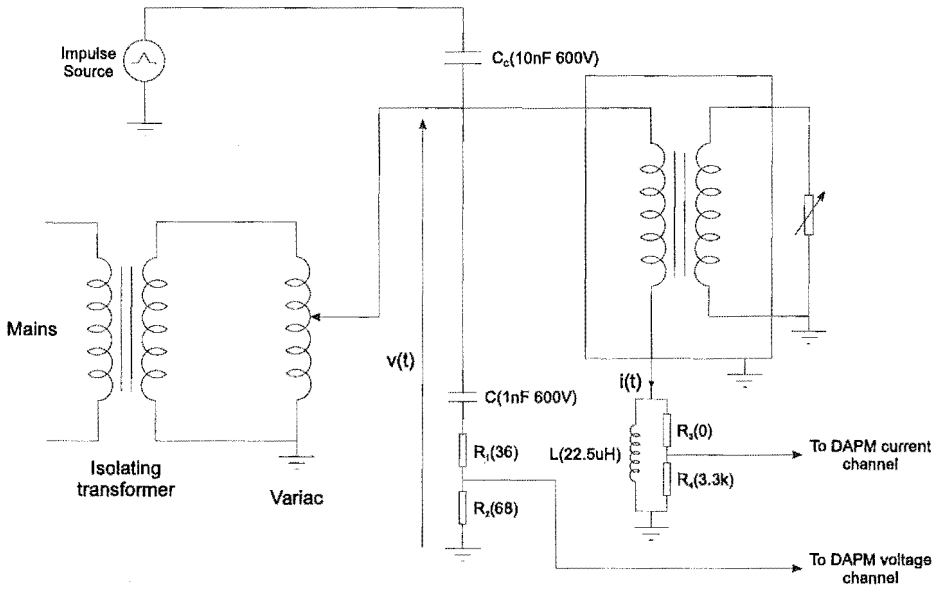


Figure 7.31 On-line test setup

$$\frac{220 \cdot 10^3}{10^{90/20}} = 6.9\text{V} \tag{7.11}$$

to the DAPM. By applying a higher order filter, the effect of any supply voltage can be attenuated into insignificance.

In 4.4.2 the reactance of the RL shunt at 50Hz is calculated to be 7.1mΩ. Thus for a 100MVA 220kV/11kV transformer operating at full load, the 50Hz voltage drop across the RL shunt would be

$$(100 \cdot 10^6 / 220 \cdot 10^3) \cdot 7.1 \cdot 10^{-3} = 3.2\text{V} \tag{7.12}$$

Minor adjustments to the transducers would easily see the voltages in Eqs. (7.11) and (7.12) reduced sufficiently to prevent the 50Hz supply from occupying more dynamic range than the signals being digitised.

It is necessary to supply the transformer with an isolated 50Hz supply. Failing to do so connects the ground reference in the test setup to the mains neutral. Because the neutral is connected to ground at the substation, then a large ground loop is setup. A large area ground loop has emfs induced in it due to time varying flux linkage (from power system currents, EM radiation etc.) which cause errors in the measurement system. See Figure 4.27 for the ground connections between the different instruments within the TICMS.

Separate isolated supplies are required in Figure 7.31 for the IGM and the transformer supply. Attempting to supply the transformer with the IGM supply will put a ground

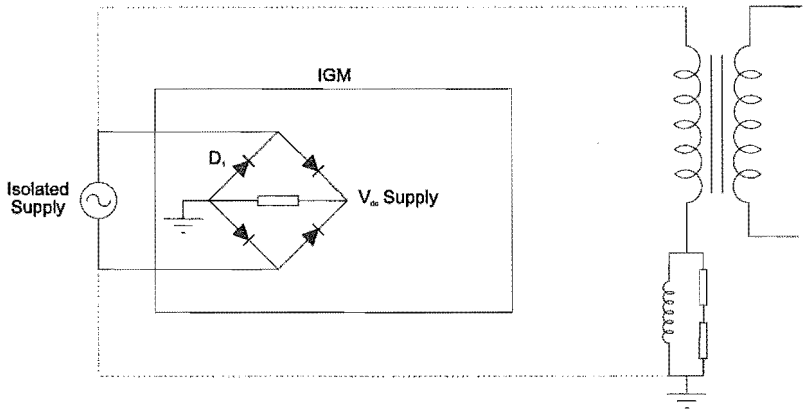


Figure 7.32 IGM and TUT supplies

connection on both sides of the bridge rectifier in the IGM (the load side consisting of a rectifying capacitor and bleed resistor, is grounded so that a ground referenced impulse is produced for use with the DAPM), as shown in Figure 7.32. This will short the supply during the negative part of the cycle, causing a short circuit current to flow through D_1, which will destroy the bridge.

7.4.1 Tests Synchronised to the 50Hz Cycle

The Test Synchroniser Module (TSM) (not shown in Figure 7.31) is an instrument that is used to synchronise the application of an impulse from the IGM to a point in the 50Hz supply cycle. This allows test sets to be conducted that can determine if the level of core magnetization has any measurable effect on the transadmittance function. Additional details on the TSM hardware can be found in 4.3.

For the synchronisation tests, the TUT had a supply voltage of 185V and a 10A load connected. Figure 7.33 compares the off-line transadmittance function with that with the impulse synchronised to point 2. Pole height reductions result when the transformer is energised as a result of changes to the self and mutual inductances of the winding. The inductance changes are a result of the change in core magnetization.

Figure 7.35 shows the transadmittance function magnitude of Tx_1 with the impulse synchronised to points 3, 5, 7, and 13 respectively. These points correspond to the indicated number of anti-clockwise turns of the TSM pot from it's fully adjusted clockwise position. From Table 4.1, the positions correspond to -0.32ms, -1.33ms, -2.27ms, -3.57ms, and -5ms with respect to a positive going zero-crossing respectively. This range extends from the negative peak to just below the positive going zero-crossing. Differences appear between the transadmittance functions in Figure 7.35 and that in Figure 7.33 b) as the transformer is energised in the former case.

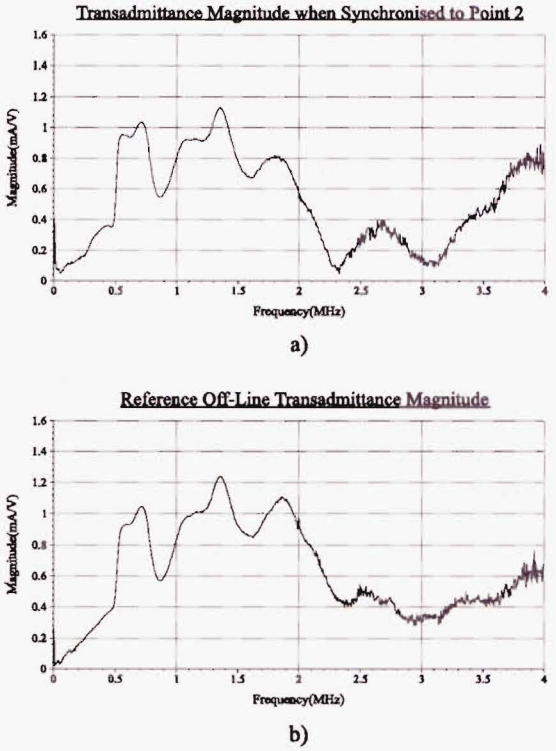


Figure 7.33 a) Synchronised to point 2 b) Off-line reference

Small differences are seen between the transadmittance functions in Figure 7.35. Differences are highlighted in Figure 7.34 showing the 1.8MHz pole for -0.32ms and -2.27ms synchronisation times. The difference can be explained by considering that the changing core magnetization causes the self and mutual inductances within the winding to vary on a cyclic basis. Small changes in the transadmittance function occur at high frequencies as the inductance changes are small. These small changes are a consequence of the core not being fully magnetized by the low voltage supply. When testing a fully energised transformer in service, more dramatic transadmittance function changes may be expected as larger changes in the magnitude of the core magnetization take place over the 50Hz cycle. Further testing needs to be done to quantify these effects.

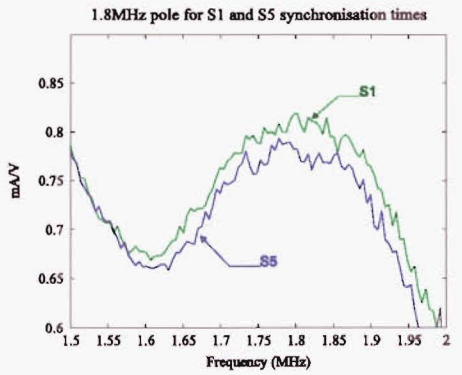


Figure 7.34 Changes in the 1.8MHz pole at -0.32ms and -2.27ms

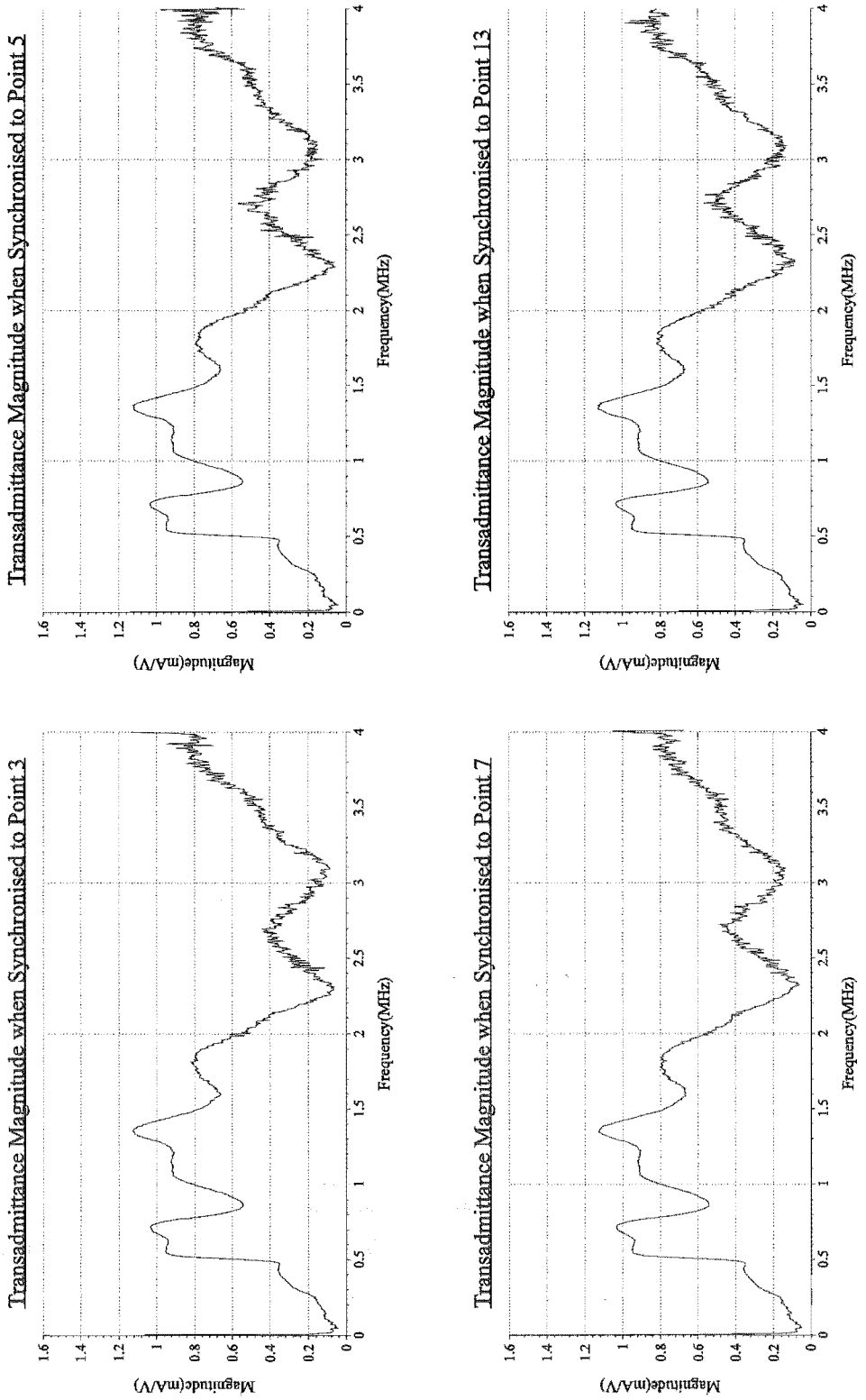


Figure 7.35 Transadmittance function with impulse synchronised to points 3, 5, 7, and 13

Hysteresis effects further limit the changes in the core magnetization over the part of the cycle that the TSM operates over. The severity of this limitation is dependent on the shape of the hysteresis loop. Figure 7.36 illustrates this concept by showing a typical hysteresis loop, the section over which the TSM may operate and the corresponding change in core

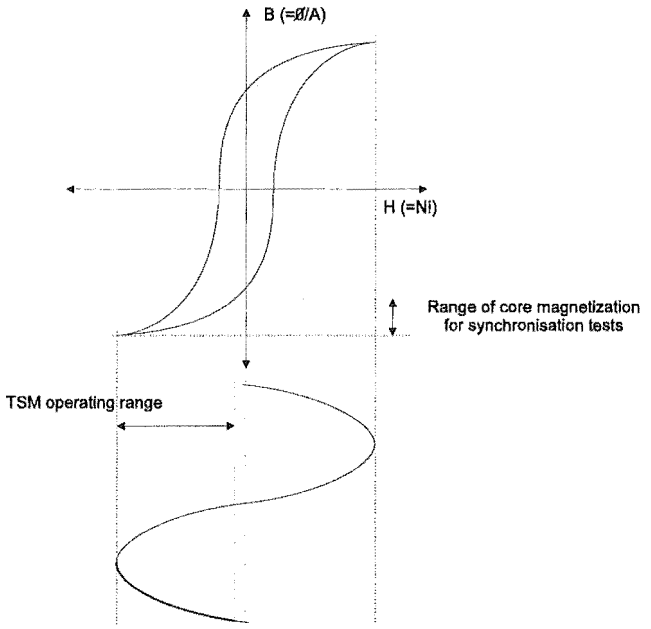


Figure 7.36 Core magnetization change over TSM operating range

magnetization. Figure 7.36 is only intended for illustration purposes. The actual range of core magnetization may differ from that shown as the transformer was not fully energised and the TSM was synchronised with respect to the supply voltage which is out of phase with the supply current. This phase difference is dominated by the transformer's load reactance. TSM hardware modifications will be needed when testing a fully energised transformer so that results over the full range of core magnetization can be recorded.

7.4.2 Effect of Load Current

To evaluate the effect of load current, the TICMS was used to determine the transadmittance function with different loads connected. For each load the TUT was supplied with 185V and testing was synchronised to point 13, i.e. the negative crest of the 50Hz cycle. Figure 7.37 illustrates the transadmittance functions resulting from load currents of 1A, 5A, and 10A. The three transadmittance functions are also plotted on the same axis over the region of maximum change where it can be seen that increasing the load current from 1A decreases the amplitude of the poles at 1.35MHz and 1.8MHz. The decreases can be attributed to the increase in core magnetization that results with the higher load currents, which in turn leads to an increase in the self and mutual inductances within the winding and a corresponding change in the transadmittance function. This mechanism is consistent with that used to explain the decrease in pole height in Figure 7.34. To further support the validity of the core magnetization mechanism, further load current tests need to be performed, involving synchronising to different points in the 50Hz cycle. Figure 7.38 shows the transadmittance function differences. Sharp differences appear at 500kHz.

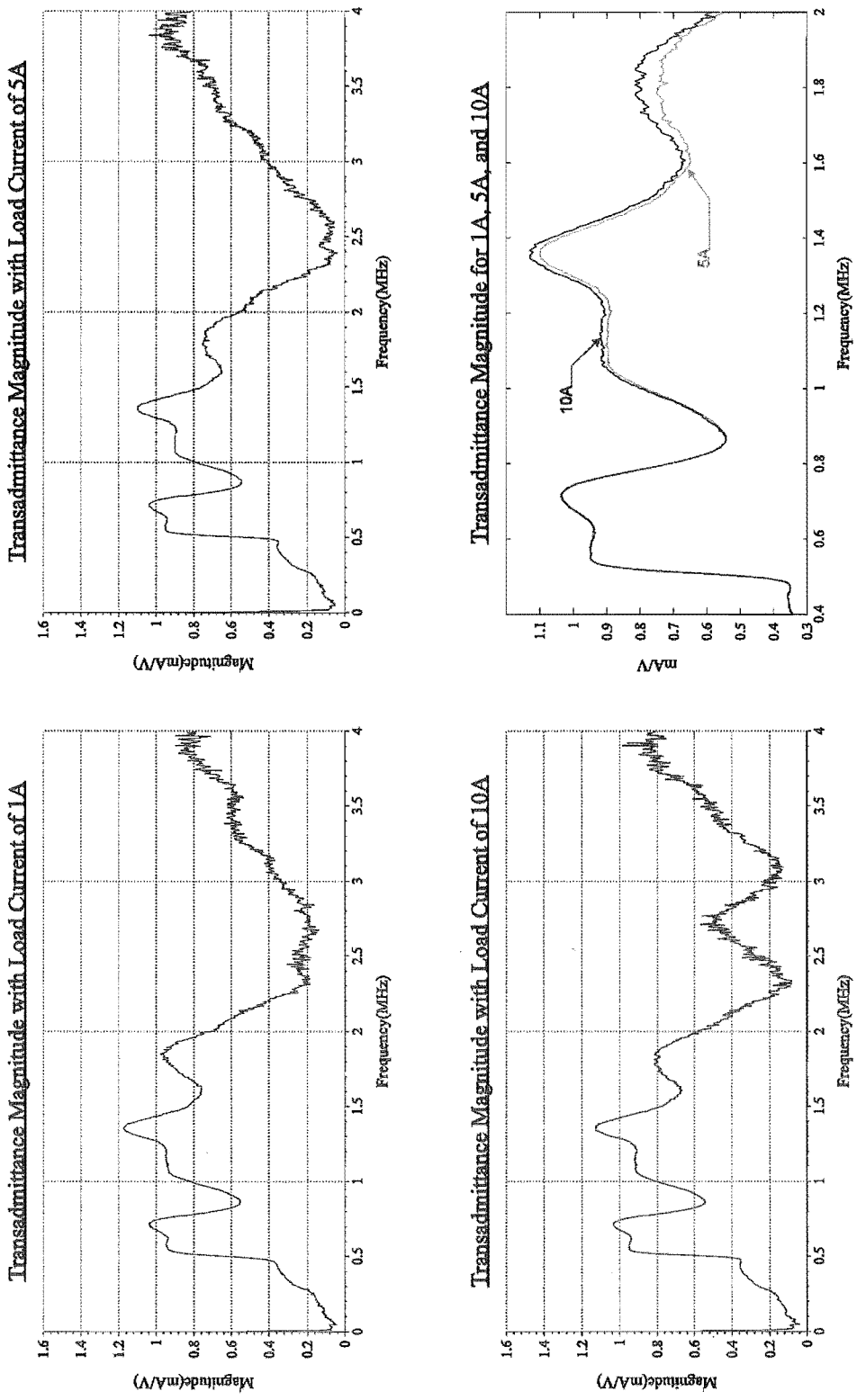


Figure 7.37 Transadmittance function with load currents of 1A, 5A, and 10A

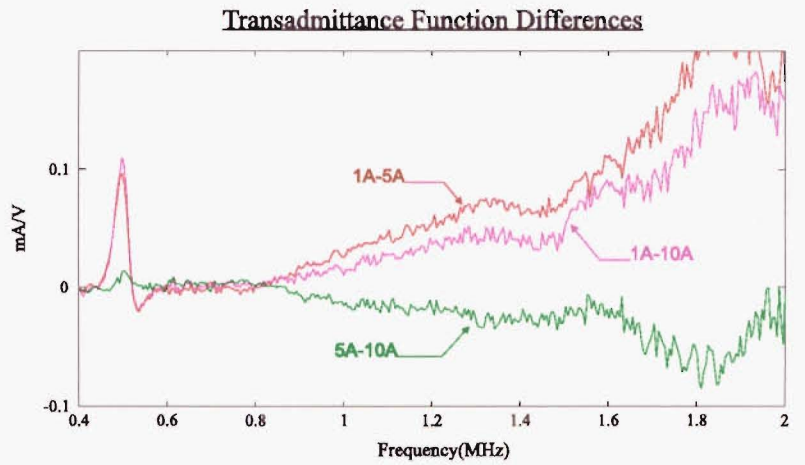


Figure 7.38 Transadmittance function differences

7.4.3 *Effect of Supply Voltage*

The transadmittance function of Tx_1 was determined at different supply voltages. When the supply voltage was increased, the load was adjusted to keep the load current constant at 1A. All tests were synchronised to the negative crest of the 50Hz supply cycle. Figs 7.39, 7.40, and 7.41 show significant differences beyond 1.5MHz. In an on-line system in the field, an additional transducer maybe needed that monitors the supply voltage for change. This is needed as the current power system configuration (e.g. the driving transformer's tap changer position) will effect the supply voltage amplitude.

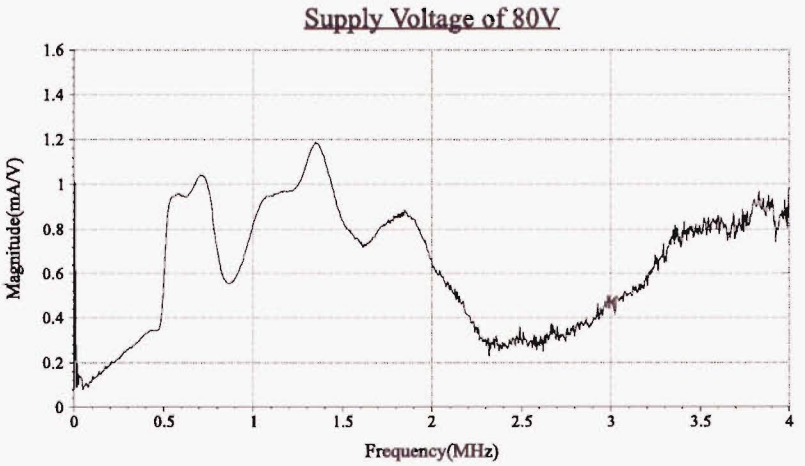


Figure 7.39 Transadmittance function magnitude of Tx_1 with a supply voltage of 80V

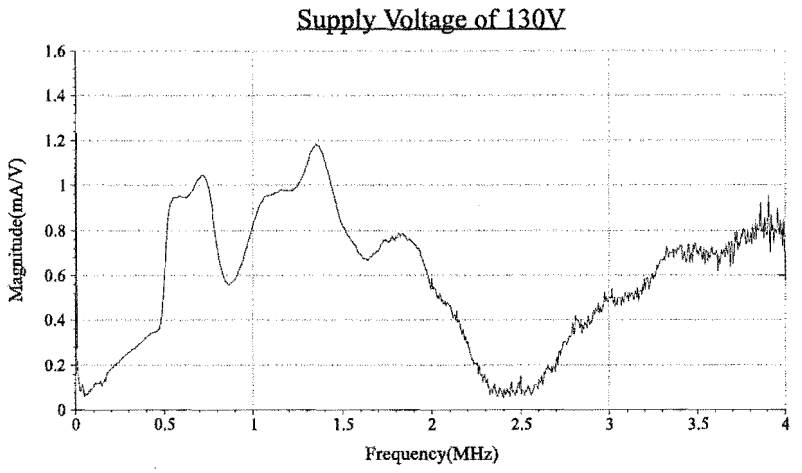


Figure 7.40 Transadmittance function magnitude of Tx_1 with a supply voltage of 130V

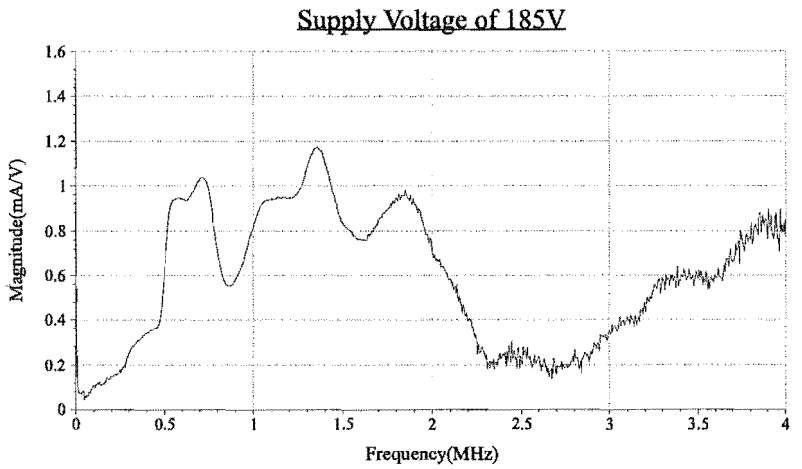


Figure 7.41 Transadmittance function magnitude of Tx_1 with a supply voltage of 185V

7.5 Conclusions

Artificial faults have been placed in the winding of the 7.5kVA transformer to establish relationships between the location and size of the fault and the corresponding changes in the transadmittance function. Sets of tests have been conducted to evaluate the effect of fault size, fault location, the introduction of simulated partial discharges, and single turn faults. The ability of the system to detect single turn faults is a key feature as this allows faults to be detected before they can snowball into catastrophic failures. The transadmittance function has been independently evaluated through the use of a time consuming sweep frequency test.

The effect of temperature on the location and height of poles in the transadmittance function of a 7.5kVA 11kV/220V distribution transformer has been established through the

use of the TICMS. Temperature results have revealed that an additional analog input is needed during on-line testing to separate temperature induced transadmittance function changes from those brought about by winding insulation faults. Additional on-line testing has been performed to evaluate the effect of supply voltage magnitude, load current magnitude, and the point in the 50Hz AC cycle when the insulation test is initiated.

7.6 References

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Chapter 8

CONCLUSIONS

A high speed data acquisition and processing system has been designed to evaluate power transformer winding insulation condition by determining the transadmittance function. The theoretical framework, design, and experimental testing of the system has been presented. The system described is the latest to evolve from the research activities of the author at the University of Canterbury and differs from existing systems in that it suppresses the large magnitude low frequency components allowing the effective dynamic range of the measuring system to be extended, extends the transadmittance function bandwidth to 3MHz enabling shorts between individual turns in an EHV transformer to be detected [1], employs a novel transducer arrangement allowing on-line measurements to be made, applies a high-speed DSP to calculate the transadmittance function in real-time.

The signal processing principles used to determine the winding transadmittance function have been presented. A powerful floating point DSP has been used to implement these signal processing operations in real-time as the research is aimed at using the system to perform on-line testing. This enables the evaluation of the winding insulation condition while the transformer is in service, allowing a faulty transformer can be taken out of service before failure takes place. On-line real-time transadmittance function evaluation has been implemented by capacitively coupling the low voltage excitation used by the TICMS onto the transformers sinusoidal input. On-line measurement of the current response is achieved through the use of an RL shunt which has been designed to have negligible reactance at 50Hz. An RC high pass filter is used to attenuate the large magnitude low frequency components of the input impulse, thus preventing them from occupying too much of the system dynamic range. Signal processing algorithms are used in the DAPM application software to restore the attenuated signal components, leading to an increase in the effective number of bits for the digitisation process. During on-line testing, the RC filter and RL shunt are also used to attenuate the large 50Hz components, preventing them from taking up any dynamic range when testing an energised transformer. As a result no additional digital signal processing is needed during on-line testing. Additional front-end hardware

development may be needed when testing transformers in service as the instrumentation system will be exposed to high frequency noise from other sources in the power system.

Artificial faults have been placed in the winding of the 7.5kVA transformer to establish relationships between the location and size of the fault and the corresponding changes in the transadmittance function. Sets of tests have been conducted to evaluate the effect of fault size, fault location, the introduction of simulated partial discharges, and single turn faults. The ability of the system to detect single turn faults is a key feature as this allows faults to be detected before they can snowball into catastrophic failures. The key issue in using this technique for identifying insulation condition changes is to be able to identify both gradual and/or sudden changes in the frequency signature. Consequently the exact or absolute value of the transadmittance function is not as important as being able to identify differential changes in the transadmittance function both in the long and short term. It is however important to have a high degree of confidence that the signatures obtained are a reasonable representation of the transadmittance function. This has been established by performing an independent evaluation through the use of a time consuming sweep frequency test.

The effect of temperature on the location and height of poles in the transadmittance function of a 7.5kVA 11kV/220V distribution transformer has been established through the use of the TICMS. Temperature results have revealed that an additional analog input is needed during in service testing to separate temperature induced transadmittance function changes from those brought about by winding insulation faults. Additional on-line testing has been performed to evaluate the effect of supply voltage magnitude, load current magnitude, and the point in the 50Hz AC cycle when the insulation test is initiated. This information allows the system to compare successive transadmittance functions and generate an alarm signal if insulation condition degradation is found to have taken place. Thus the system will eventually become a 'black box' that permanently sits beside a transformer continuously evaluating insulation condition.

At present low voltage impulse testing is being used to determine the transadmittance function both off-line and on-line. Field trials which involve testing a fully energised transformer in service are currently being planned. The system is also being extended to allow natural disturbances and power system transients to be used as an excitation source. This will allow the initiation of a test upon the arrival of a transient.

The following is a summary of the key contributions made by this thesis to the state-of-the-art in power transformer insulation condition monitoring:

- The suppression of large magnitude low frequency components to increase the effective

dynamic range of the measuring system. This makes it possible to perform the necessary high frequency measurements and extend the transadmittance function bandwidth to 3MHz. Extending the bandwidth to 3MHz makes it possible to detect breakdown between adjacent turns in an EHV transformer [1]. Previous attempts have determined the transadmittance function to around 1.5MHz and have not been able to detect breakdown between individual turns.

- The application of a complex FFT algorithm that is able to transform both the current and voltage channels into the frequency domain simultaneously. This was achieved by forming a complex time domain function and using a sorting procedure after the FFT to extract the voltage and current spectra. This approach increases the computational efficiency of the TICMS and enables the transadmittance function to be calculated at a higher rate in real-time. This increase in speed allows increased real-time averaging to be performed, leading to improved accuracy at higher frequencies.
- Novel transducer designs that allow the TICMS to interface to a fully energised power transformer while it is in service. As a result on-line measurements can be made and the transadmittance function monitored on a continuous basis.
- The calculation of the transadmittance function in real-time through the application of a high speed DSP with on-chip hardware support for fast and efficient numerical processing operations. On-line real-time calculation enables winding insulation faults to be detected early and potentially catastrophic failures prevented. The TICMS is unique in that it allows the transadmittance function to be determined to 3MHz in real-time for an in service power transformer. The pioneering work of Malewski and Poulin [1] involved calculating the transadmittance function in an offline situation over a period of minutes using pre-recorded data.
- The ability of the system to detect different types of faults by analysis of the changes in the transadmittance function signatures caused by these faults under different conditions has been demonstrated. Most important it has been shown that faults between individual turns can be detected. This is a significant contribution as faults between individual turns can quickly deteriorate leading to total transformer failure.
- The effects of temperature, load current, supply voltage, and core magnetization on the transadmittance function of a 7.5kVA 11kV/220V single phase distribution transformer have been investigated. Test results have revealed the need for additional TICMS analog inputs for monitoring temperature and tap changer position.

In support of the above the following two papers have been accepted for publication in the *IEEE Transactions on Power Delivery*:

- **A Transformer Insulation Condition Monitoring System**

- **The Application of Signal Processing Techniques to Determine a Wideband Transadmittance Function of a Power Transformer Winding**

A copy of each paper is included in Appendix H. Two additional papers are planned. One is a review paper covering current research in fault detection, diagnosis and transformer insulation conditioning monitoring. The second planned paper addresses the application of the TICMS and presents the findings detailed in Chapter 7.

8.1 Future Research

Chapter 7 discussed the introduction of artificial faults to a 7.5kVA 11kV/230V single phase distribution transformer. The transformer was disassembled and known faults were added. The TICMS was used to evaluate the effect of these faults on the winding transadmittance function. Knowing the effect of a fault allows that fault to be detected when a given change is observed in the transadmittance function. However as was detailed in Chapter 7 this technique requires that a transformer identical to that being protected be disassembled and internally altered. Because such alterations may make the transformer unsuitable for service this approach can be costly.

An alternative approach is to develop a high frequency model (up to 3MHz) for the transformer winding under test. Once developed, the model could be used in a SPICE simulation to determine the model transadmittance function. The measured transadmittance function can then be used to check the accuracy of that determined from the model. The differences could be used to further refine the model if necessary. Once a suitable model has been developed, the affect of artificial faults can be evaluated by simulation.

A high frequency transformer winding model may possess the following attributes:

- The winding inductance and core magnetisation should dominate the low frequency behaviour of the model while the winding capacitance should dominate the high frequency behaviour.
- Because the core magnetisation is a function of frequency, the self and mutual inductances included in the model may be a function of frequency. However as the frequency is increased and the magnetisation drops, the winding capacitance will become dominant.
- When a winding section is shorted the core magnetisation is weakened (reducing self and mutual inductances) and losses increase due to the eddy currents flowing in the shorted winding section. The effects may be negligible for small and single turn faults.
- Skin effect may need to be taken into consideration over the frequency range of interest.

A high frequency winding model has the following advantages:

- Enables a wide range of fault conditions to be evaluated including the simultaneous presence of more then one fault.
- An expensive power transformer does not to be sacrificed for testing purposes.
- Enables the transient voltage distribution over the winding to be determined by simulation. This information allows the transformer manufacturer to place more insulation at places of higher stress.

To develop an accurate high frequency model of a transformer winding the following issues need to be addressed

- How the characteristics of the magnetic circuit change with increasing frequency
- Modeling of the parasitic capacitances that have an effect over the frequency range of interest (up to 3MHz)
- Modeling of the mutual couplings within the winding that have an effect over the frequency range of interest
- The distributed circuit nature of the winding at the frequencies of interest (up to 3MHz)

Further, different transformers have different winding constructions which will impact the model.

8.2 Future TICMS Developments

Currently the TICMS excites the TUT with a low voltage impulse supplied via the IGM. Power transformers are continuously exposed to system generated and natural transients arising from switching operations and lightening strikes respectively. Such transients can supply the necessary excitation required to determine the transadmittance function. A system based on this approach can be achieved by re-designing the front end of the TICMS. However the unknown characteristics of the incoming transients add the following complications to the required design modification:

- **Unknown spectra:** Because it is not known whether or not the incoming transient has spectral components above the Nyquist limit, anti-alias filters are needed. The use of low pass anti-alias filters require that higher sampling rate A/D converters be used to accommodate the filter transition band.
- **Unknown amplitude:** Not knowing the transient amplitude makes it difficult to have the data acquisition subsystem performing optimally. If the attenuated transients that are

digitised exceed the analog input voltage range of the A/D converters, an erroneous transadmittance function will result. If too much attenuation is employed the A/D converter quantisation noise will reduce the frequency to which the transadmittance function can be determined. The use of a non-linear logarithmic attenuator may be useful here.

- **Unknown duration:** For practical reasons, transients can only be recorded at high sampling rates for a finite time duration. If the time length of the transient being digitised exceeds the time window of the TICMS then truncation results. This requires the recorded data to be windowed and can introduce errors into the transadmittance function evaluation process.

Further difficulties associated with the use of system generated and natural transients include:

- Surge arrestors are used in power systems to divert potentially harmful transients. Using these transients as an excitation source exposes the transformer's insulation to additional stresses that may affect the service life of the transformer.
- The frequency of occurrence of transients with adequate spectral characteristics may mean that the required transfer function is determined on an infrequent basis.

The waveshape of the impulse produced by the IGM is controlled to produce an impulse with the desired spectral characteristics as discussed in Chapter 4. The concern was to ensure that the supplied excitation had sufficient high frequency components to allow the transadmittance function to be determined to 3MHz. If the supplied impulse could be modulated so as to shift it's spectra to a frequency band of interest then the affect of system noise on the transadmittance function at high frequencies could be reduced. Further the frequency to which the transadmittance function can be determined could be extended according to the limits of the data acquisition system. Such a modulation can be achieved by employing an overdamped RLC circuit to generate the transformer excitation. By suitably adjusting passive component values, the decay rate and center frequency of the RLC response could be controlled. DAPM outputs along with application software could be used to automate the adjustment process.

In Chapter 7 the effect of temperature on the transadmittance function was investigated. Here it was seen that temperature had a measurable effect on the transadmittance function of a 7.5kVA 11kV/220V single phase distribution transformer. For future on-line testing in the field, additional DAPM analog inputs will be needed to monitor temperature, transformer tap changer position and load current. Further as more experience is gained with its use, the system needs to be used to build up and maintain a database for each

individual transformer construction type.

8.3 Concluding Remarks

Many different techniques for fault detection, fault diagnosis and transformer insulation condition monitoring have been presented in Chapters 2 and 3. Many of these techniques have been used for many years and their practice is well established while others are still being further developed through current research activities. Even though the use of these techniques continues to provide the power system engineer with invaluable information, there are shortcomings and limitations as power transformer failures are still taking place regularly around the world. The transadmittance function method is unlikely to be the one and only used method of the future for on-line diagnosis. Rather it will be used together with existing methods such as DGA to enrich what the power system engineer already has available.

The methods presented in Chapters 2 and 3 are used to identify transformer fault conditions before they deteriorate to a severe state. All of the methods presented require some experience in order to correctly interpret the observations. Researchers have applied artificial intelligence concepts in order to encode these techniques. Many of these attempts have concentrated on only a single diagnostic technique and have failed to fully manage the inherent uncertainty in the various methods [2]. A better analysis would result by aggregating transadmittance function results returned by the TICMS with information from many of these techniques. These results would contribute to enrich the ability of the transadmittance function approach as an excellent tool for conditioning monitoring by locating faults in power transformers.

Fuzzy-sets and expert systems have been used to formulate various rules for transformer fault diagnosis [3]. A knowledge base rule or a fuzzy membership function is selected based on past experience. The reliability of the diagnosis increases with the amount of information available from previous tests. Therefore the knowledge base required can be large and complex. Very complex systems can be characterised with very little explicit knowledge using artificial neural networks (ANNs). The ANN method has been used to reveal the hidden relationships between fault types and dissolved gases through a training process [4][5][6]. The relationship between transadmittance function changes and fault conditions could be learned by an ANN from actual experience (through training samples). Obvious and not so obvious (hidden) relationships can be detected by the ANN and used to develop it's basis for interpretation of transadmittance function data. Through a training process, an ANN can reveal complex mechanisms that may be unknown to experts. In

contrast, expert and fuzzy-set systems can only use explicit knowledge to select knowledge base rules and fuzzy membership functions. Theoretically an ANN could represent any observable phenomenon.

During laboratory evaluation of the TICMS, an attached PC was used to command the device and to display the received transadmittance function results. However ultimately the system will become a 'black box' that sits permanently besides a transformer continuously evaluating insulation condition. The detection of slow changes in the transadmittance function will facilitate the application of improved maintenance scheduling for the power transformer, which is a key item of capital equipment in a power system. The detection of rapid changes in the transadmittance function will provide an increased level of protection for the power transformer. This will be achieved by activating an alarm condition to the power system operator so that action can be taken to avoid a catastrophic transformer failure.

It will obviously take several years of trail use and further refining the accuracy of the predictions on the remaining life of the transformer insulation, before reaching the final objective of automatic prediction of transformer failure by specialized software. There is undoubtedly further work to do in order to reach this objective but the potential power of such an instrument would make the effect very worthwhile.

8.4 References

[1] Malewski R., Poulin B., **Impulse Testing of Power Transformers using the Transfer Function Method**, *IEEE Transactions on Power Delivery*, Vol. PWRD-3, No. 2, pp. 476-489, April 1988

[2] Tomsovic K., Tapper M., Ingvarsson T., **A Fuzzy Information Approach to Integrating Different Transformer Diagnostic Methods**, *IEEE Transactions on Power Delivery*, Vol. 8, No. 3, July 1993

[3] Lin C.E., Ling J.M., Huang C.L., **An Expert System for Transformer Fault Diagnosis using Dissolved Gas Analysis**, *IEEE Transactions on Power Delivery*, Vol. 8, No. 1, Jan 1993

[4] Zhang Y., Ding X., Liu Y., Griffin P.J., **An Artificial Neural Network Approach to Transformer Fault Diagnosis**, *IEEE Transactions on Power Delivery*, Vol. 11, No. 4, Oct 1996

[5] Ding X., Yao E., Liu Y., Griffin P.J., **ANN Based Transformer Fault Diagnosis Using Gas-In-Oil Analysis**, *57th American Power Conference*, Chicago IL, April 1995

[6] Bhattacharyya S.K., Smith R.E., Haskew T.A., **A Neural Network Approach to Transformer Fault Diagnosis using Dissolved Gas Analysis Data**, *NAPS*, 1993

Appendix A

SOFTWARE MODELS

An implementation independent software model for the DAPM application software is presented. The model consists of data-flow diagrams, a data dictionary, and activity specifications.

A.1 DAPM Software

A.1.1 Data-flow Diagrams

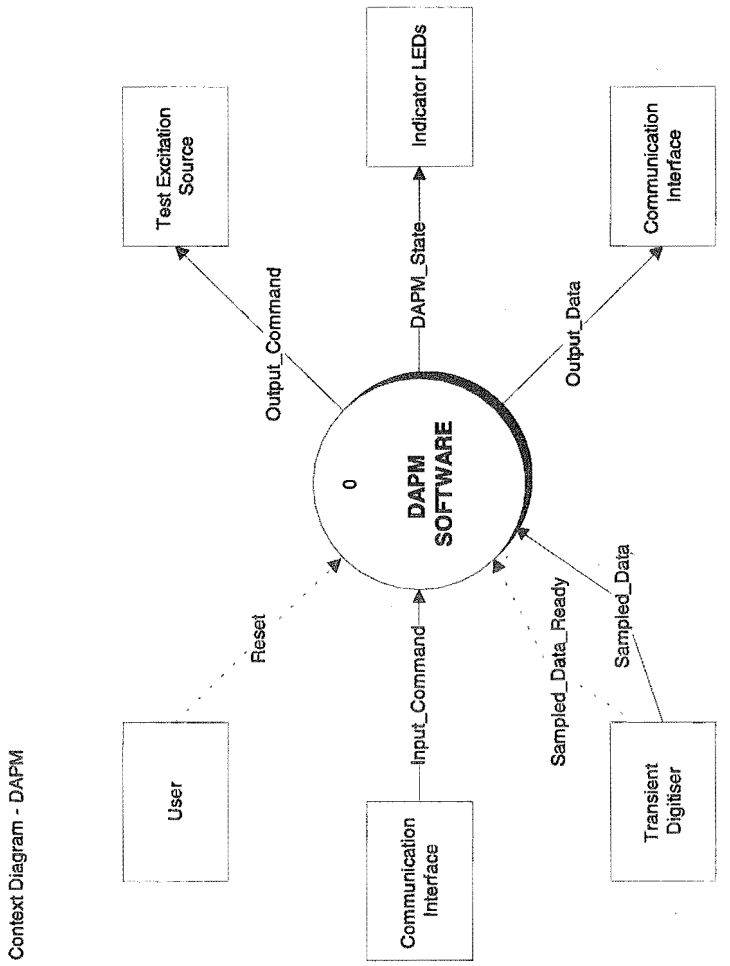


Figure A.1 Context Diagram - DAPM

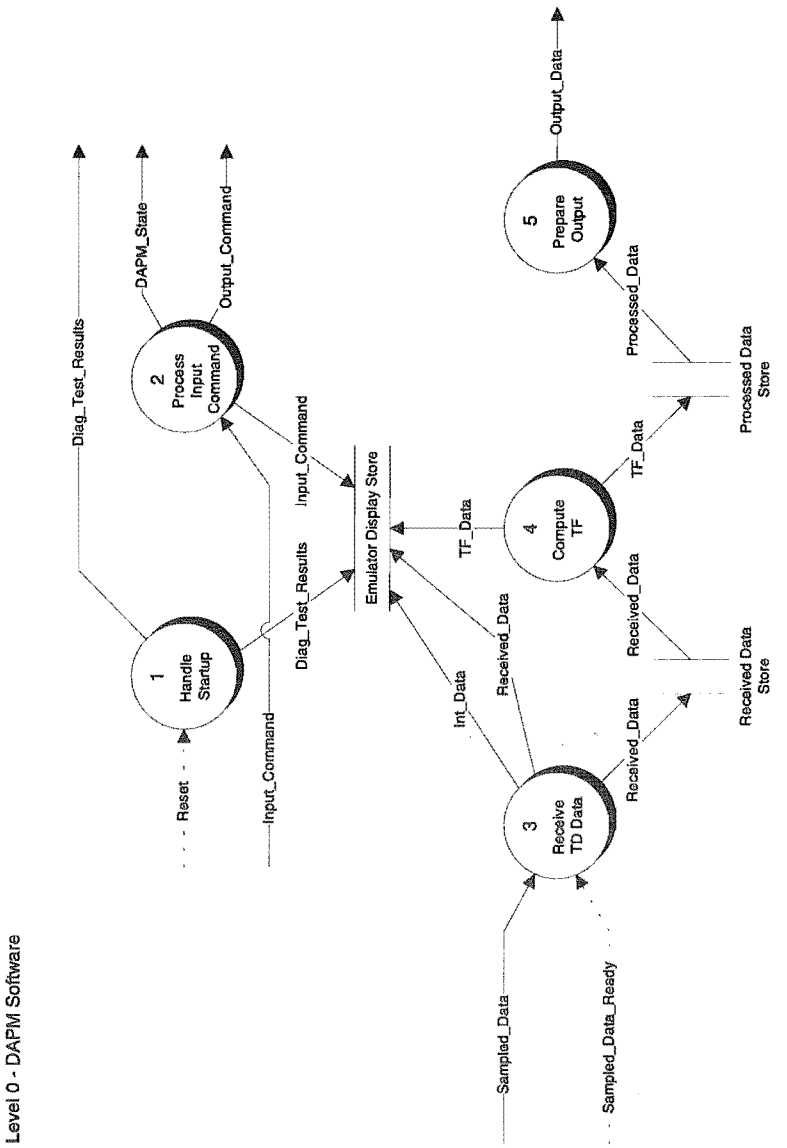


Figure A.2 Level 0 - DAPM Software

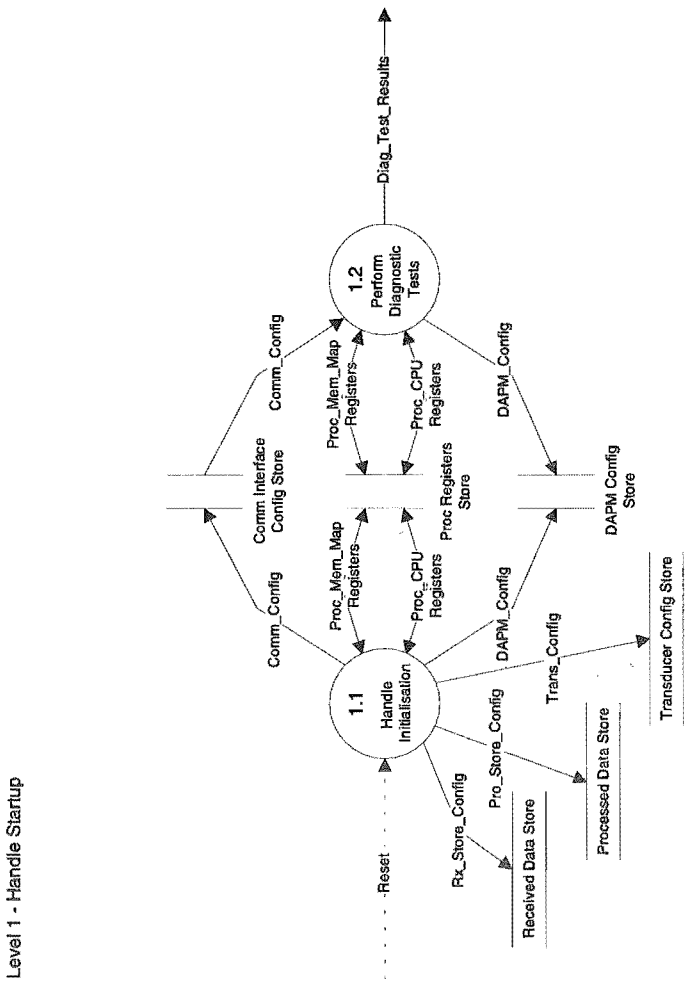


Figure A.3 Level 1 - Handle Startup

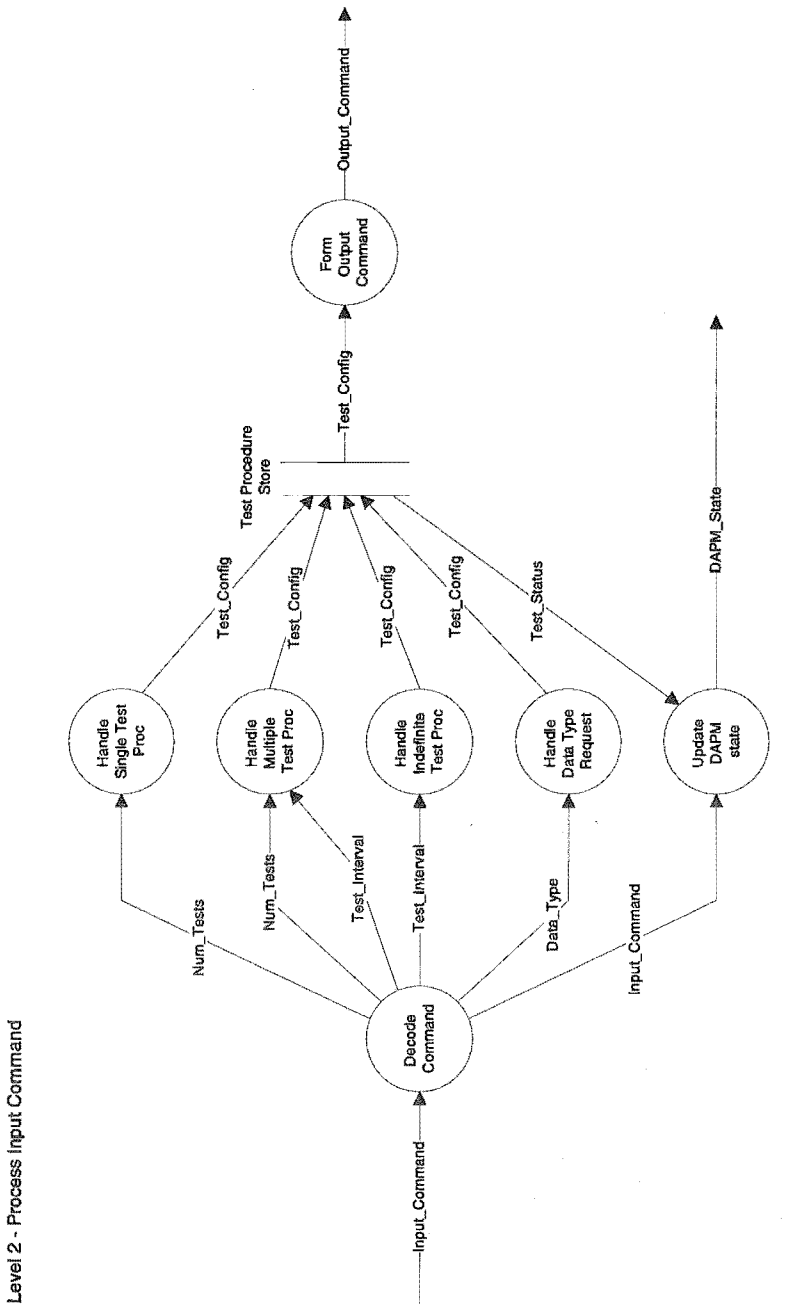


Figure A.4 Level 2 - Process Input Command

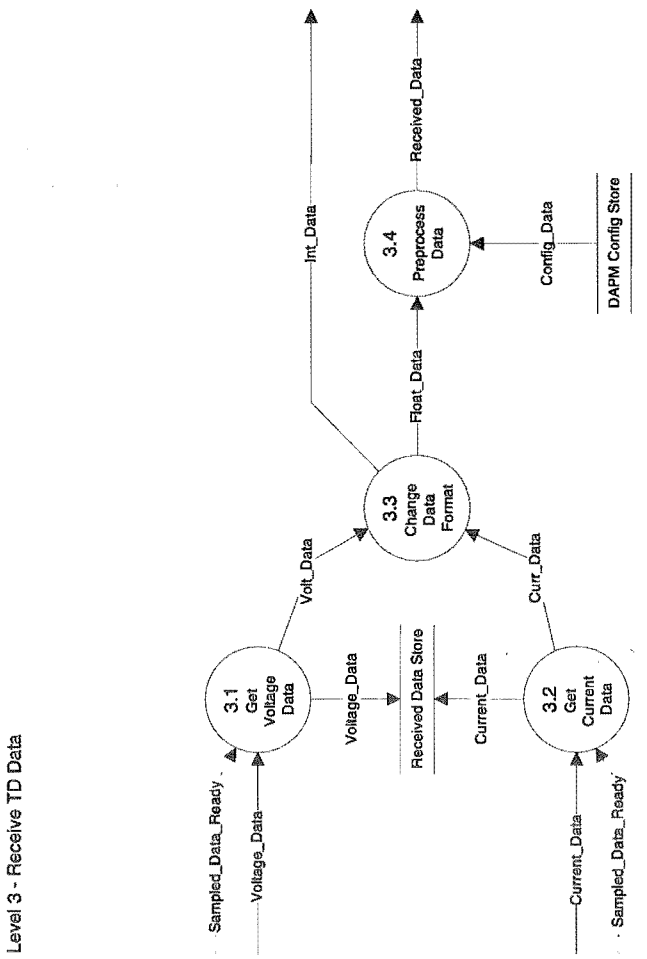


Figure A.5 Level 3 - Receive TD Data

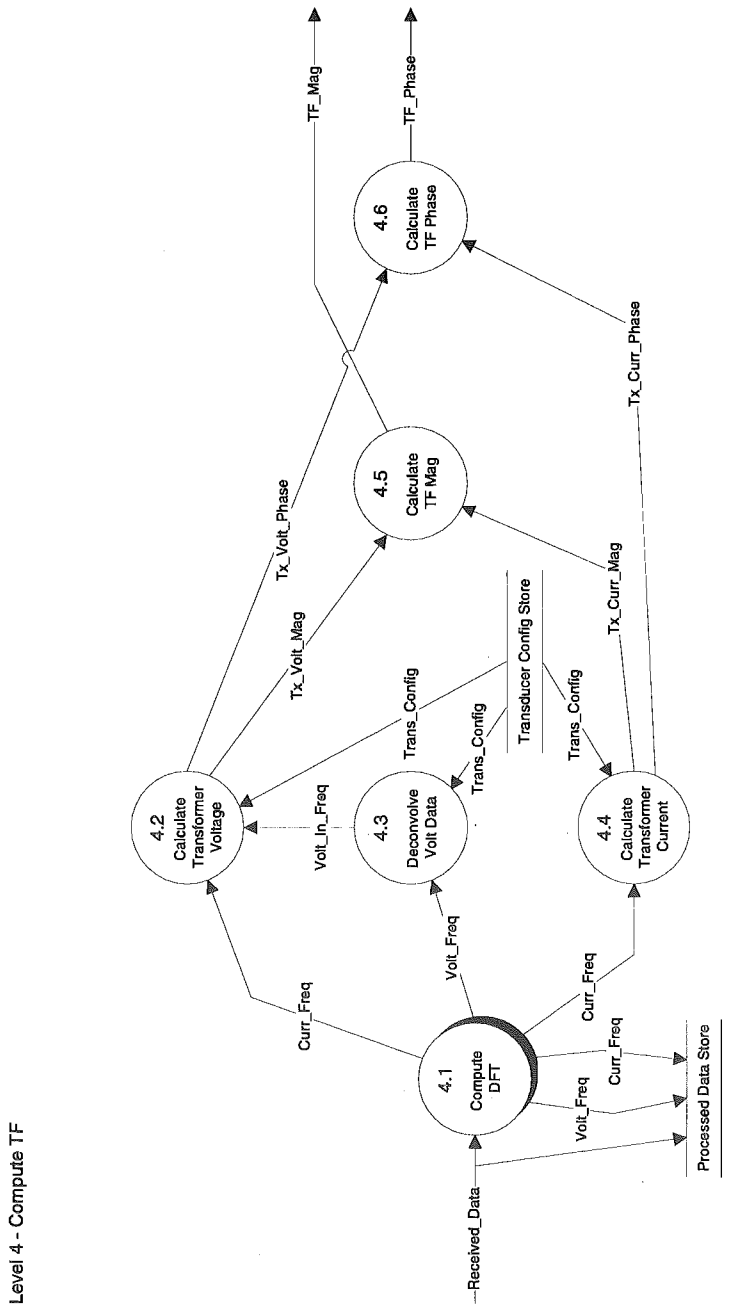


Figure A.6 Level 4 - Compute TF

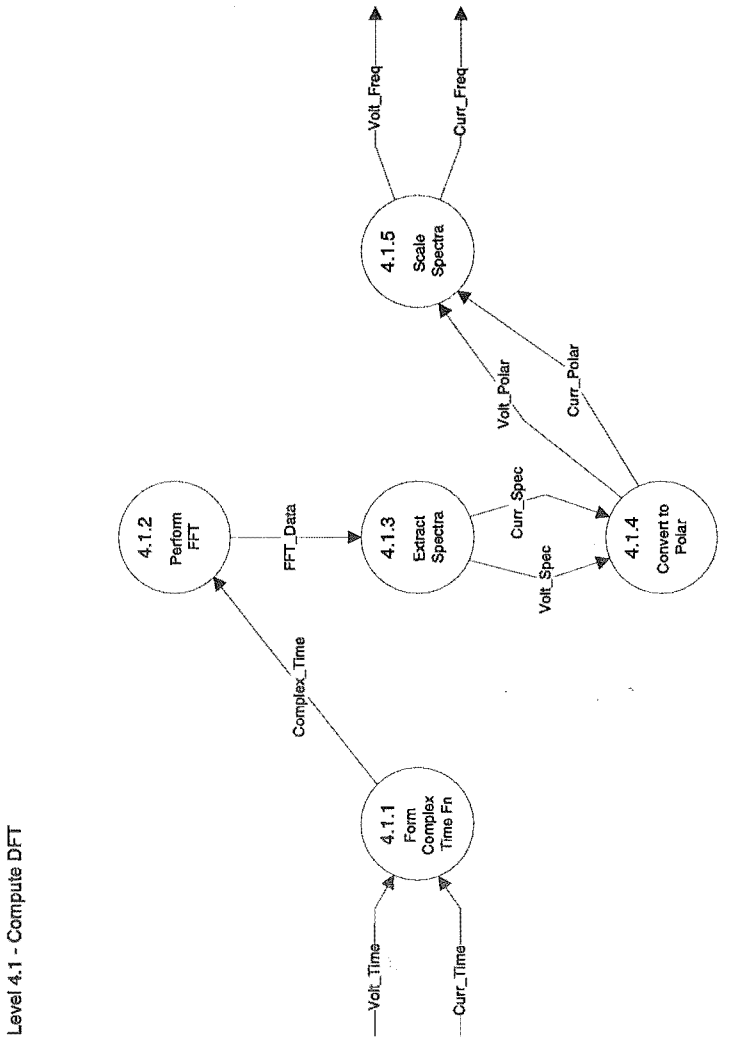


Figure A.7 Level 4.1 - Compute DFT

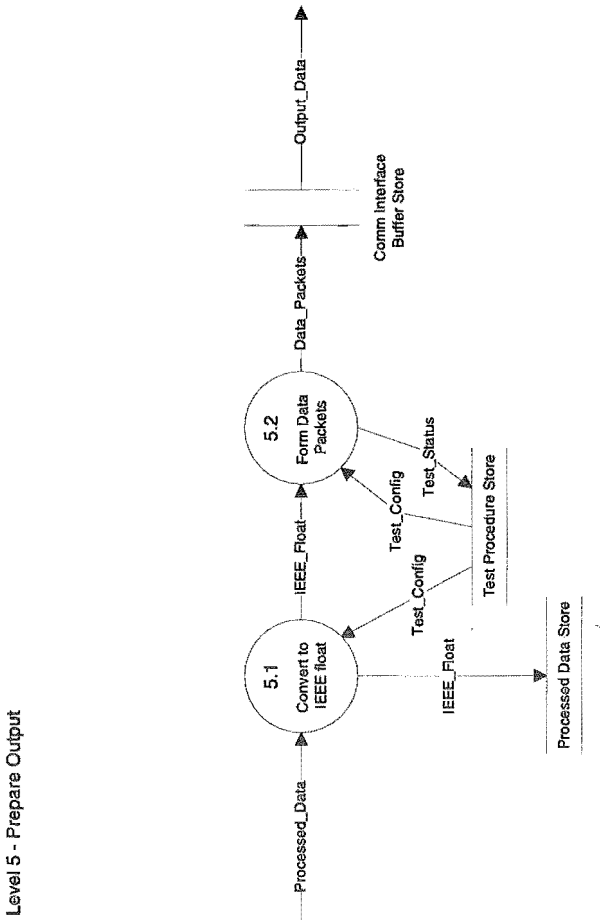


Figure A.8 Level 5 - Process Output

A.1.2 Data Dictionary

Data Flow Items

adc_int = sign + $\{bit\}_{11}^{11}$
12-bit signed 2's complement integer data format from transient digitiser.

address = $\{bit\}_{24}^{24}$

bit = 0 | 1

bus_cycle_reg = processor_int
Target processor register used to set the number of bus cycle wait-states and to put the bus into the high impedance state.

busy = bit
Used to indicate if the DAPM is in the process of executing a user input command.

capture_all_first = bit
A user option that gets the DAPM to capture and process all test data before transmitting any display.

cap_value = $\{digit\}_{3}^{5}$
Capacitance measured in pF.

Comm_Config = data_tx_rate + error_detect + packet_size
Data needed to initialise the communication interface between the DAPM and the attached PC.

comm_pass = bit
Indicates if the communication interface diagnostic test passed.

Complex_Time = $\{processor\_float\}_{num\_points}^{num\_points}$ + $\{processor\_float\}_{num\_points}^{num\_points}$
Complex-time function with real and imaginary parts set to Volt_Time and Curr_Time respectively.

compress = bit
A user option that gets the DAPM to compress data before being transmitted to the attached PC.

Config_Data = zero_pad_ratio + volt_atten + curr_atten + volt_dc + curr_dc
Configuration data that allows software to remove any DC offset on either channel, remove attenuation needed to couple power transformer signals to the DAPM and to zero pad the captured data.

curr_afae = $\{digit\}_{1}^{3}$
AF/AE offset vector for current channel FIFO buffer.

curr_atten = processor_float
Total analog attenuation in current channel.

curr_buffer_size = 1024 | 2048

Effective current FIFO buffer size in bytes.

Curr_Data = $\{adc\_int\}_{num\_samples}^{num\_samples}$
Current data transferred from the transient digitiser after floating data bus bits have been reset to zero.

curr_dc = processor_float
Analog DC offset on current channel.

Current_Data = $\{adc\_int\}_{num\_samples}^{num\_samples}$
Raw current channel data transferred from the transient digitiser.

curr_float = $\{processor\_float\}_{num\_samples}^{num\_samples}$
curr_int converted to target processors 32-bit floating point data format.

Curr_Freq = curr_mag + curr_phase
Polar format of frequency domain description of Curr_Time.

curr_imag = $\{processor\_float\}_{num\_points}^{num\_points}$
Imaginary part of complex Curr_Spec.

curr_int = $\{processor\_int\}_{num\_samples}^{num\_samples}$
Curr_Data converted to target processors 32-bit signed integer data format.

curr_mag = $\{processor\_float\}_{num\_points}^{num\_points}$
Magnitude spectrum of Curr_Time.

curr_phase = $\{processor\_float\}_{num\_points}^{num\_points}$
Phase spectrum of Curr_Time.

Curr_Polar = unscaled_curr_mag + curr_phase
Unscaled polar format of frequency domain description of Curr_Time.

curr_real = $\{processor\_float\}_{num\_points}^{num\_points}$
Real part of complex Curr_Spec.

Curr_Spec = curr_real + curr_imag
Rectangular format of frequency domain description of Curr_Time.

Curr_Time = $\{processor\_float\}_{num\_points}^{num\_points}$
curr_float with DC offset removed, analog attenuation removed and zero padding.

curr_trans = res_value + ind_value
Current channel transducer component values.

DAPM_Config = Config_Data + volt_afae + curr_afae
DAPM configuration data used in digital signal processing calculations.

DAPM_State = ready | busy
Indicates to the user if the DAPM is able to receive a command or not.

Data_Packets = $\{packet\}^{16}$
The maximum number of packets that the communication interface buffer is capable of holding.

data_tx_rate = $\{digit\}_4^6$
Data transfer rate of the communication interface in kbits/s. Minimum and maximum values are 1200 and 115200 respectively.

Data_Type = type_volt_time + type_curr_time + type_volt_mag + type_volt_phase + type_curr_mag + type_curr_phase + type_tf_mag + type_tf_phase
The data types that are to be transmitted to the attached PC for display, as requested by the user.

Diag_Test_Results = volt_afae + curr_afae + volt_dc + curr_dc + ram_pass + comm_pass
The result of each diagnostic test run by the DAPM at startup.

digit = 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9

dma_regs = $\{processor\_int\}_1$
Target processor register used to set up DMA controller.

error_detect = bit
Determines if error detection is used over communication interface.

exponent = $\{bit\}_8^8$
8-bit exponent of target processors 32-bit floating point data format.

FFT_Data = real + imag
Frequency domain description of Complex_Time.

Float_Data = volt_float + curr_float
Captured time domain data in targets processors 32-bit floating point data format.

ieee_exponent = $\{bit\}_8^8$
8-bit exponent of IEEE single precision floating point data format.

IEEE_Float = $\{ieee\_single\_pre\}_{512}^{16384}$
Processed_Data after it has been converted to IEEE single precision floating point data format. Minimum value corresponds to positive frequencies of a single data type when 1024 points are used. Maximum value corresponds to all data when 2048 points are used.

ieee_mantissa = $\{bit\}_{23}^{23}$
23-bit mantissa of IEEE single precision floating point data format.

ieee_sign = bit
Sign bit of IEEE single precision floating point data format.

ieee_single_pre = ieee_sign + ieee_exponent + ieee_mantissa
IEEE single precision floating point data format.

imag = $\{processor\_float\}_{num\_points}^{num\_points}$
Imaginary part of complex FFT_Data.

ind_value = $\{digit\}_1^3$
Inductance measured in uH.

infinite = Data_Type + Test_Interval + compress
Test parameters when insulation tests are being performed on a continuous basis.

initialise_to_zero = bit
Determines if data storage locations are initialised to zero at startup.

Input_Command = Data_Type + Num_Tests + Test_Interval + capture_all_first + compress
User command sent from PC application software to DAPM.

Int_Data = volt_int + curr_int
Captured time domain data in targets processors 32-bit signed integer data format.

interrupt_regs = $\{processor\_int\}_1$
Target processors registers used to set up interrupt structure.

int_sign = bit
Sign bit of target processors 32-bit signed integer data format.

i/o_regs = $\{processor\_int\}_1$
Target processors registers used to configure its I/O ports.

mantissa = $\{bit\}_{23}^{23}$
23-bit mantissa of target processors 32-bit floating point data format.

multiple = Data_Type Num_Tests + Test_Interval + capture_all_first + compress
Test parameters when multiple insulation tests are performed from a single command.

num_points = 1024 | 2048
The number of voltage and current time domain data points that are processed by the DAPM software.

num_samples = 1024 | 2048
The number of time domain samples captured by the transient digitiser.

Num_Tests = digit | 10 | 15 | 20 | 25 | 30
The number of consecutive tests requested by the user for a test procedure.

Output_Data = $\{Data\_Packets\}_{128}^{4096}$
The total number of data packets send from the DAPM to the attached PC. Minimum value corresponds to positive frequencies of a single data type when 1024 points are used. Maximum value corresponds to all data types when 2048 points are used.

Output_Command = bit
Used to activate the IGM and initiate an insulation test.

packet = $\{bit\}_8^8$
8-bit data packet that is sent over the communication interface.

packet_size = 8
Communication interface data packet size in bits.

Proc_CPU Registers = interrupt_regs + status_reg + i/o_regs
Some of the target processors CPU registers.

Processed_Data = Received_Data + Volt_Freq + Curr_Freq + TF_Data
Captured data in time and frequency domains and the transadmittance function of the transformer under test.

processor_float = exponent + sign + mantissa
Target processors 32-bit floating point data format.

processor_int = int_sign + $\{bit\}_{31}^{31}$
Target processors 32-bit signed integer data format.

Proc_Mem_Map Registers

= timer_counter_regs + dma_regs + bus_cycle_reg
Some of the target processors memory mapped registers used to control peripheral devices.

pro_size = $\{digit\}_{5}^{6}$
Size of processed data store in bytes. Minimum value is 16384 (16k) and maximum value is 122880 (120k).

Pro_Store_Config = address + pro_size + initialise_to_zero
Configuration data used to initialise the processed data store at startup.

ram_pass = bit
Indicates if the DAPM system RAM diagnostic tests passed.

ready = bit
Used to indicate that the DAPM is ready to accept a user command.

real = $\{processor\_float\}_{num\_points}^{num\_points}$
Real part of complex FFT_Data.

Received_Data = Volt_Time + Curr_Time
The captured time domain data after it has been converted to the target processors 32-bit floating point data format and preprocessed.

res_value = $\{digit\}_{1}^{5}$
Resistance measured Ω

rx_size = volt_buffer_size + curr_buffer_size
Size of received data store in bytes. Minimum value is 2048 (2k) and maximum value is 4096 (4k).

Rx_Store_Config = address + rx_size + initialise_to_zero
Configuration data used to initialise the received data store at startup.

Sampled_Data = Voltage_Data + Current_Data
Raw data from the transient digitiser.

sign = bit
Sign bit of target processors 32-bit floating point data format.

single = Data_Type + compress
Test parameters when single insulation test is performed from a single command.

status_reg = processor_int
A target processor register that contains information on its current state.

test_completed = bit
Used to indicate that the DAPM has finished executing a test procedure.

Test_Config = single | multiple | infinite
The test configuration mode that is currently in progress.

Test_Interval = 5 | 10 | 15 | 20 | 25 | 50 | 100 | 500 | 1000 | 5000 | 10000
Time between consecutive tests in a test procedure in milliseconds.

test_in_progress = bit
Used to indicate that a test procedure is in progress.

Test_Status = test_in_progress | test_completed

TF_Data = TF_Mag + TF_Phase
The transadmittance function of the transformer under test in polar format.

timer_counter_regs = $\{processor\_int\}_{1}$
Processor peripheral registers used to control timer/event counter.

Trans_Config = volt_trans + curr_trans
Transducer component values needed in digital signal processing calculations.

Tx_Curr_Mag = $\{processor\_float\}_{num\_points}^{num\_points}$
Magnitude spectrum of transient current signal through transformer.

Tx_Curr_Phase = $\{processor\_float\}_{num\_points}^{num\_points}$
Phase spectrum of transient current signal through transformer.

TF_Mag = $\{processor\_float\}_{num\_points}^{num\_points}$
Magnitude spectrum of transformer transadmittance function.

TF_Phase = $\{processor\_float\}_{num\_points}^{num\_points}$
Phase spectrum of the transformer transadmittance function.

Tx_Volt_Mag = $\{processor\_float\}_{num\_points}^{num\_points}$
Magnitude spectrum of transient voltage signal that is applied across the transformer.

Tx_Volt_Phase = $\{processor\_float\}_{num\_points}^{num\_points}$
Phase spectrum of transient voltage signal that is applied across the transformer.

type_curr_mag = bit

Used to indicate if curr_mag is to be sent for display.

type_curr_phase = bit
Used to indicate if curr_phase is to be sent for display.

type_curr_time = bit
Used to indicate if Curr_Time is to be sent for display.

type_tf_mag = bit
Used to indicate if TF_Mag is to be sent for display.

type_tf_phase = bit
Used to indicate if TF_Phase is to be sent for display.

type_volt_time = bit
Used to indicate if Volt_Time is to be sent for display.

type_volt_mag = bit
Used to indicate if volt_mag is to be sent for display.

type_volt_phase = bit
Used to indicate if volt_phase is to be sent for display.

volt_afae = $\{\text{digit}\}_1^3$
AF/AE offset vector for voltage channel FIFO buffer.

volt_atten = processor_float
Total analog attenuation in voltage channel.

Voltage_Data = $\{\text{adc\_int}\}_{\text{num\_samples}}^{\text{num\_samples}}$
Raw voltage channel data transferred from the transient digitiser.

volt_buffer_size = 1024
Voltage FIFO buffer size in bytes.

Volt_Data = $\{\text{adc\_int}\}_{\text{num\_samples}}^{\text{num\_samples}}$
Voltage data transferred from the transient digitiser after floating data bus bits have been reset to zero.

volt_dc = processor_float
Analog DC offset on voltage channel.

volt_float = $\{\text{processor\_float}\}_{\text{num\_samples}}^{\text{num\_samples}}$
volt_int converted to target processors 32-bit floating point data format.

Volt_Freq = volt_mag + volt_phase
Polar format of frequency domain description of Volt_Time.

volt_imag = $\{\text{processor\_float}\}_{\text{num\_points}}^{\text{num\_points}}$
Imaginary part of complex Volt_Spec.

Volt_In_Freq = volt_in_mag + volt_in_phase
Polar format of frequency domain description of voltage transducer input signal.

volt_in_mag = $\{\text{processor\_float}\}_{\text{num\_points}}^{\text{num\_points}}$

Magnitude of Volt_In_Freq.

volt_in_phase = $\{processor\_float\}_{num\_points}^{num\_points}$
Phase of Volt_In_Freq.

volt_int = $\{processor\_int\}_{num\_samples}^{num\_samples}$
Volt_Data converted to target processors 32-bit signed integer data format.

volt_mag = $\{processor\_float\}_{num\_points}^{num\_points}$
Magnitude spectrum of Volt_Time.

volt_phase = $\{processor\_float\}_{num\_points}^{num\_points}$
Phase spectrum of Volt_Time.

Volt_Polar = unscaled_volt_mag + volt_phase
Unscaled polar format of frequency domain description of Volt_Time.

volt_real = $\{processor\_float\}_{num\_points}^{num\_points}$
Real part of complex Volt_Spec.

Volt_Spec = volt_real + volt_imag
Rectangular format of frequency domain description of Volt_Time.

Volt_Time = $\{processor\_float\}_{num\_points}^{num\_points}$
volt_float with DC offset removed, analog attenuation removed and zero padding.

volt_trans = $\{res\_value\}_2^2$ + cap_value
Voltage channel transducer component values.

unscaled_curr_mag = $\{processor\_float\}_{num\_points}^{num\_points}$
Magnitude of Curr_Polar.

unscaled_volt_mag = $\{processor\_float\}_{num\_points}^{num\_points}$
Magnitude of Volt_Polar.

zero_pad_ratio = 1 | 2
Used to zero pad 1024 voltage channel samples to 2048. Also used to zero pad the current channel samples from 1024 to 2048 when the DMA controller is not being used to extend the effective current channel FIFO buffer size.

Data Stores

Comm Interface Buffer = Data_Packets
A data store that buffers data packets before being sent to the attached PC.

Comm Interface Config = Comm_Config
A data store that contains setup information used to initialise the serial interface so that it compatible with the attached PC.

DAPM Config = DAPM_Config
A data store that contains DAPM hardware setup and signal processing configuration information needed to calculate the transadmittance

function.

Emulator Display = Diag_Test_Results + Input_Command + Int_Data + Received_Data + TF_Data

A data store that contains information that can be conveyed to the user during system development. This data store is used to verify that software subsystems are operating correctly.

Processed Data = Processed_Data

A data store that contains captured and processed data in their final form on the target system.

Received Data = Received_Data

A data store that contains captured time domain data after it has preprocessed.

Test Procedure = Test_Config

A data store that contains the command information sent from the attached PC, as specified by the PC operator.

Transducer Config = Trans_Config

A data store that contains transducer hardware information needed to calculate the transadmittance function from the test setup.

Appendix B

DAPM SOFTWARE ABSTRACTIONS

Data and procedural abstractions used during the DAPM application software design are presented.

B.1 Data Abstractions

complex = **data type is** *ComplexAdd, ComplexMult, GetReal, GetImag, SetReal, SetImag, ComplexVectorAdd, ComplexVectorMult, ConvPolar*

Overview

complex consists of two ordered real numbers representing the real and imaginary parts respectively

Operations

ComplexAdd = **proc** (a: complex, b: complex) **returns** (sum: complex)

requires none

modifies none

effects on return the real and imaginary parts of sum are the sum of the real and imaginary parts of a and b respectively

ComplexMult = **proc** (a: complex, b: complex) **returns** (product: complex)

requires none

modifies none

effects on return the real and imaginary parts of product are $(a_r b_r - a_i b_i)$ and $(a_r b_i + a_i b_r)$ respectively where a_r, b_r, a_i, and b_i are the real and imaginary parts of a and b

GetReal = **proc** (a: complex) **returns** (re: real)

requires none

modifies none

effects on return re is the real number used to represent the real

part of a

GetImag = **proc** (a: complex) **returns** (im: real)

requires none

modifies none

effects on return im is the real number used to represent the imaginary part of a

SetReal = **proc** (a: complex, re: real)

requires none

modifies a

effects on return the real part of a is equal to re

SetImag = **proc** (a: complex, im: real)

requires none

modifies a

effects on return the imaginary part of a is equal to im

ComplexVectorAdd = **proc** (a: array[complex], b: array[complex]) **returns** (sum: array[complex])

requires a and b must contain the same number of array elements

modifies none

effects array elements from a and b with the same array position are input to the ComplexAdd operation and the result is placed into the same array position in sum. The procedure is applied to all array element pairs in a and b

ComplexVectorMult = **proc** (a: array[complex], b: array[complex]) **returns** (product: array[complex])

requires a and b must contain the same number of array elements

modifies none

effects array elements from a and b with the same position are input to the ComplexMult operation and the result is placed into the same array position in product. The procedure is applied to all array element pairs in a and b

ConvPolar = **proc** (a: complex) **returns** (b: polar)

requires none

modifies none

effects the data type a is converted to polar and the result is returned in b

polar = **data type is** *PolarMult, GetMag, GetPhase, SetMag, SetPhase, ConvRect*

Overview

polar consists of two ordered real numbers representing the magnitude and phase respectively

Operations

PolarMult = **proc** (a: polar, b: polar) **returns** (product: polar)

requires none

modifies none

effects on return the magnitude of product is equal to the product of the magnitudes of a and b, and the phase of product is equal to the sum of the phases of a and b

GetMag = **proc** (a: polar) **returns** (mag: real)

requires none

modifies none

effects on return mag is equal to the magnitude part of a

GetPhase = **proc** (a: polar) **returns** (ph: real)

requires none

modifies none

effects on return ph is equal to the phase part of a

SetMag = **proc** (a: polar, mag: real)

requires none

modifies a

effects on return the magnitude of a is equal to mag

SetPhase = **proc** (a: polar, ph: real)

requires none

modifies a

effects on return the phase of a is equal to ph

ConvRect = **proc** (a: complex) **returns** (b: complex)

requires none

modifies none

effects the data type a is converted to complex and the result is returned in b

IEEEFloat = **data type is** *ConvToIEEE*, *ConvVectorToIEEE*

Overview

IEEEFloat is the 32-bit IEEE single precision floating-point format used to represent real numbers on a PC

Operations

ConvToIEEE = **proc** (a: real) **returns** (b: IEEEFloat)

requires the data type of a to be in the native floating-point format of

the target hardware

modifies none

effects the data type a is converted to IEEEFloat and the result is returned in b

ConvVectorToIEEE = **proc** (a: array[real]) **returns** (b: array[IEEEFloat])

requires the data type of the elements of a to be in the native floating-point format of the target hardware

modifies none

effects the data type of the elements of a are converted to complex and the results are returned in the elements of b

B.2 Procedural Abstractions

UnwrapPhase = **proc** (a: array[polar])

requires none

modifies a

effects on return the phase of a is 'unwrapped' by adding or subtracting multiples of 2π to the phase of array elements so that 2π 'jumps' are not seen between the phases of consecutive array elements

Appendix C

SCREEN CAPTURES

Additional screen captures taken of the TICMS Windows application software that were not presented in Chapter 6 are given. Included are the screen captures illustrating the following features:

- **Windows Metafile:** Figure C.1 shows the dialog box that allows the user to save the contents of a selected display window as a Windows Metafile
- **Voltage and Current:** Figure C.2 and Figure C.3 show the voltage and current display windows respectively
- **Voltage and Current Magnitudes:** Figure C.4 and Figure C.5 show the voltage magnitude and current magnitude display windows respectively

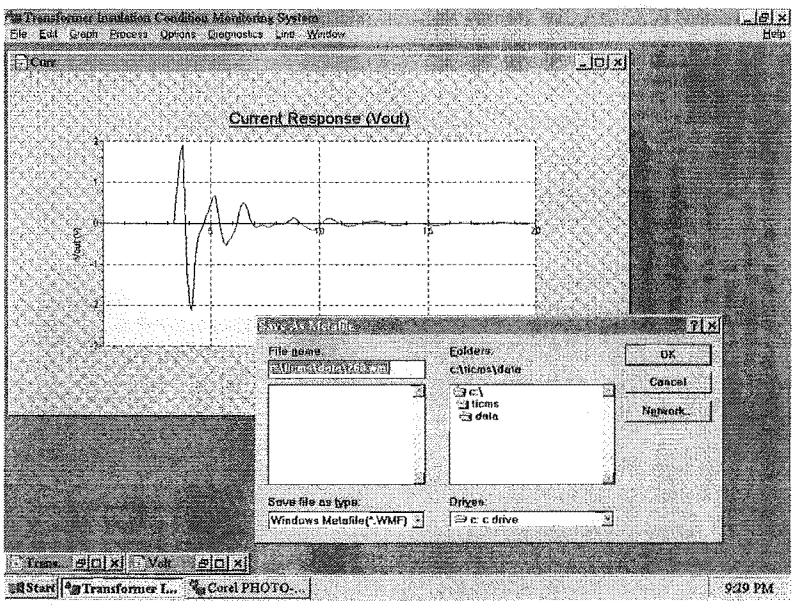


Figure C.1 Windows Metafile saving option

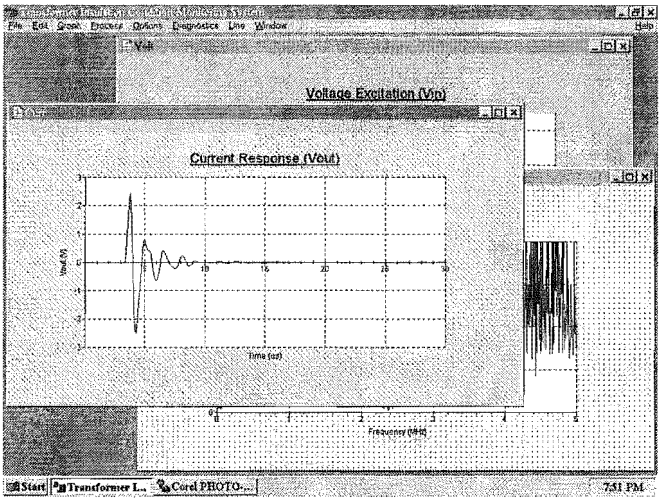


Figure C.2 Voltage display window

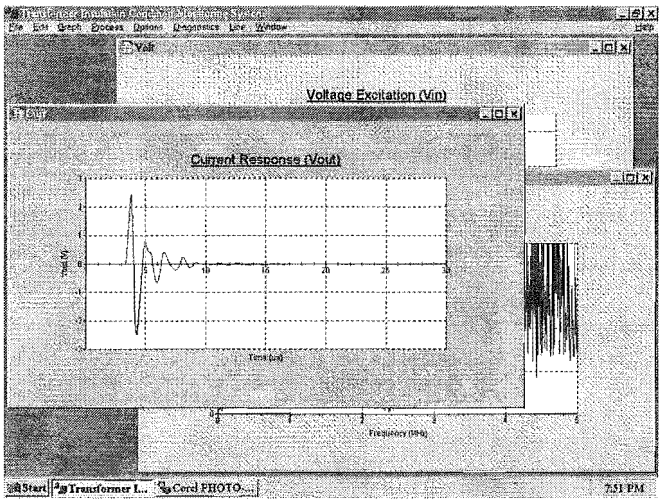


Figure C.3 Current display window

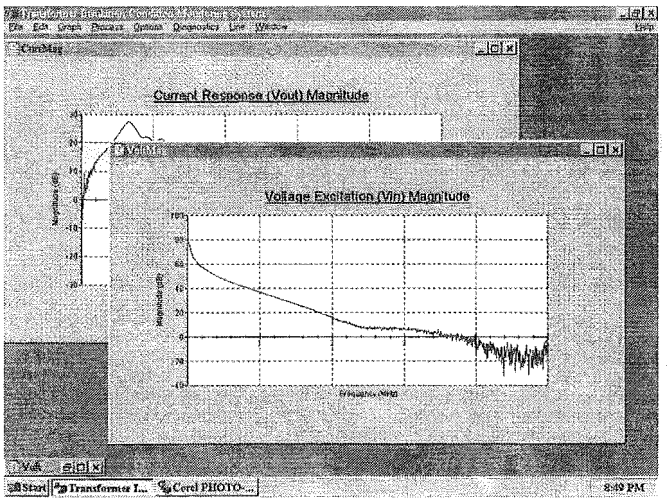


Figure C.4 Voltage magnitude display window

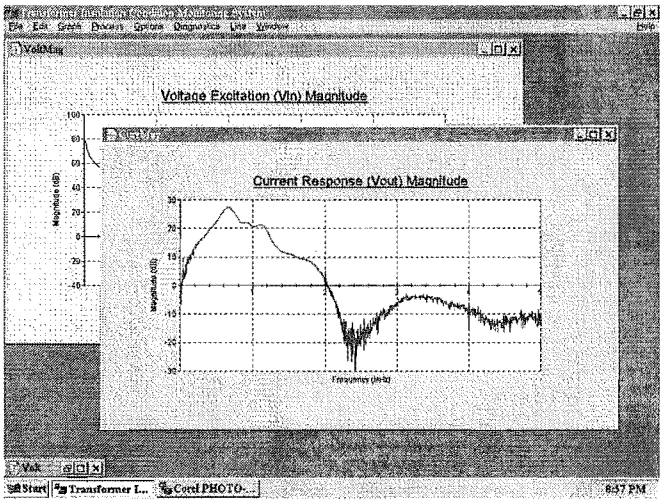


Figure C.5 Current magnitude display window

Appendix D

IMPULSE GENERATOR ANALYSIS

The Laplace transform is used to analyze the impulse generator circuit used in the IGM. An expression is developed for the output voltage in terms of the circuit's RC values. The solution is then manipulated to allow circuit values to be determined in terms of the rise and fall times of the impulse. Finally an expression is developed that is used to evaluate the efficiency of a given circuit implementation.

D.1 Laplace Analysis

The impulse generator circuit and its Laplace equivalent for the instant when the switch is closed are shown in Figure D.1. The Laplace transform of the output voltage $V_{out}(s)$ is determined as follows

$$V_{out}(s) = \frac{I_{out}(s)}{C_2 s} \tag{D.1}$$

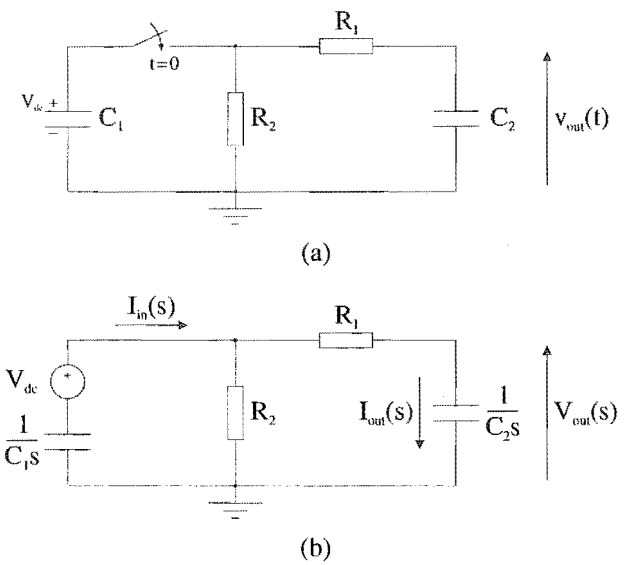


Figure D.1 (a) Impulse generator circuit (b) Laplace equivalent circuit

where

$$I_{out}(s) = \frac{R_2 I_{in}(s)}{R_1+R_2+1/C_2 s} \tag{D.2}$$

and

$$I_{in}(s) = \frac{V_{dc}/s}{\frac{1}{C_1 s}+\frac{R_2(R_1+1/C_2 s)}{R_1+R_2+1/C_2 s}} \tag{D.3}$$

Substituting Eqs. (D.2) and (D.3) into Eq. (D.1) and simplifying produces

$$V_{out}(s) = \left(\frac{R_2 V_{dc}}{((R_1+R_2)C_2 s+1)s}\right) \Big/ \left(\frac{1}{C_1 s}+\frac{(R_1 C_2 s+1)R_2}{(R_1+R_2)C_2 s+1}\right) \tag{D.4}$$

which is further simplified to

$$V_{out}(s) = \frac{R_2 C_1 V_{dc}}{(R_1+R_2)C_2 s+1+(R_1 C_2 s+1)R_2 C_1 s} \tag{D.5}$$

Writing the denominator of Eq. (D.5) as a quadratic in s produces

$$V_{out}(s) = \frac{R_2 C_1 V_{dc}}{R_1 R_2 C_1 C_2 s^2+((R_1+R_2)C_2+R_2 C_1)s+1} \tag{D.6}$$

Dividing the numerator and denominator by the coefficient of s^2 produces

$$V_{out}(s) = \frac{V_{dc}/R_1 C_2}{s^2+((R_1 C_2+R_2 C_2+R_2 C_1)/R_1 R_2 C_1 C_2)s+1/R_1 R_2 C_1 C_2} \tag{D.7}$$

Letting $-\alpha_1$ and $-\alpha_2$ denote the roots of the quadratic denominator allows Eq. (D.7) to be rewritten as

$$V_{out}(s) = \frac{V_{dc}/R_1 C_2}{(s+\alpha_1)(s+\alpha_2)} = \frac{A}{(s+\alpha_1)}+\frac{B}{(s+\alpha_2)} \tag{D.8}$$

Combining the terms in the RHS of Eq. (D.8) produces

$$V_{out}(s) = \frac{A(s+\alpha_2)+B(s+\alpha_1)}{(s+\alpha_1)(s+\alpha_2)} \tag{D.9}$$

The partial fraction terms A and B are next determined by equating coefficients in Eqs. (D.8) and (D.9) so that

$$A+B=0 \tag{D.10}$$

and

$$\alpha_2 A+\alpha_1 B=\frac{V_{dc}}{R_1C_2} \tag{D.11}$$

Solving Eqs. (D.10) and (D.11) for A and B allows Eq. (D.8) to be rewritten as

$$V_{out}(s)=\frac{V_{dc}/(R_1C_2(\alpha_2-\alpha_1))}{(s+\alpha_1)}+\frac{V_{dc}/(R_1C_2(\alpha_1-\alpha_2))}{(s+\alpha_2)} \tag{D.12}$$

Taking the inverse Laplace transform of Eq. (D.12) and simplifying produces the desired result

$$v(t)=\frac{V_{dc}}{R_1C_2(\alpha_2-\alpha_1)}\left[e^{-\alpha_1 t}-e^{-\alpha_2 t}\right] \tag{D.13}$$

D.2 Circuit Implementation

Expressing α_1 and α_2 in terms of R_1, R_2, C_1, and C_2 allows a circuit implementation to be derived for a given impulse waveshape. First the quadratic formula is used to express the roots of the quadratic denominator in Eq. (D.7) as follows

$$-\alpha_1,-\alpha_2=\frac{-\left(\frac{R_1C_2+R_2C_2+R_2C_1}{R_1R_2C_1C_2}\right)\pm\sqrt{\left(\frac{R_1C_2+R_2C_2+R_2C_1}{R_1R_2C_1C_2}\right)^2-\frac{4}{R_1R_2C_1C_2}}}{2} \tag{D.14}$$

which is manipulated to produce

$$-\alpha_1,-\alpha_2=\frac{-(R_1C_2+R_2C_2+R_2C_1)}{2R_1R_2C_1C_2}\pm\sqrt{\frac{(R_1C_2+R_2C_2+R_2C_1)^2-4R_1R_2C_1C_2}{4(R_1R_2C_1C_2)^2}} \tag{D.15}$$

Further simplification yields

$$-\alpha_1,-\alpha_2=-\frac{1}{2}\left(\frac{1}{R_1C_1}+\frac{1}{R_1C_2}+\frac{1}{R_2C_1}\right)\pm\sqrt{\frac{1}{4}\left(\frac{1}{R_1C_1}+\frac{1}{R_1C_2}+\frac{1}{R_2C_1}\right)^2-\frac{1}{R_1R_2C_1C_2}} \tag{D.16}$$

so that

$$\alpha_1,\alpha_2=\frac{a}{2}\mp\sqrt{\left(\frac{a}{2}\right)^2-b} \tag{D.17}$$

where

$$a = \frac{1}{R_1C_1} + \frac{1}{R_1C_2} + \frac{1}{R_2C_1} \tag{D.18}$$

and

$$b = \frac{1}{R_1R_2C_1C_2} \tag{D.19}$$

Next α_1 and α_2 are added and subtracted to produce

$$\alpha_1 + \alpha_2 = a \tag{D.20}$$

and

$$\frac{\alpha_1 - \alpha_2}{2} = \sqrt{\left(\frac{a}{2}\right)^2 - b} \tag{D.21}$$

Substituting Eq. (D.20) into (D.21) and simplifying produces

$$b = \frac{(\alpha_1 + \alpha_2)^2 - (\alpha_1 - \alpha_2)^2}{4} \tag{D.22}$$

from which

$$b = \alpha_1\alpha_2 \tag{D.23}$$

Finally Eqs. (D.18) and (D.19) are substituted into Eqs. (D.20) and (D.23) to produce

$$\alpha_1 + \alpha_2 = \frac{1}{R_1C_1} + \frac{1}{R_1C_2} + \frac{1}{R_2C_1} \tag{D.24}$$

and

$$\alpha_1\alpha_2 = \frac{1}{R_1R_2C_1C_2} \tag{D.25}$$

Eqs. (D.24) and (D.25) allow a circuit implementation to be derived from a given impulse waveshape.

R_1 and R_2 can be expressed in terms of C_1, C_2, α_1 and α_2 by further manipulating Eqs. (D.24) and (D.25). The results are

$$R_1 = \frac{1}{2C_2}\left[\left(\frac{1}{\alpha_1}+\frac{1}{\alpha_2}\right)-\sqrt{\left(\frac{1}{\alpha_1}+\frac{1}{\alpha_2}\right)^2-\frac{4(C_1+C_2)}{\alpha_1\alpha_2C_1}}\right] \tag{D.26}$$

and

$$R_2 = \frac{1}{2(C_1+C_2)}\left[\left(\frac{1}{\alpha_1}+\frac{1}{\alpha_2}\right)+\sqrt{\left(\frac{1}{\alpha_1}+\frac{1}{\alpha_2}\right)^2-\frac{4(C_1+C_2)}{\alpha_1\alpha_2C_1}}\right] \tag{D.27}$$

D.3 Efficiency Determination

The efficiency of the impulse generator circuit in Figure D.1 is defined as follows

$$\eta = \frac{V_{peak}}{V_{dc}} \tag{D.28}$$

where V_{peak} represents the peak voltage of the impulse generated. To find V_{peak} it is necessary to set to zero the derivative of the impulse with respect to time as follows

$$\frac{dv(t)}{dt} = \frac{d}{dt}\left(\frac{V_{dc}}{R_1C_2(\alpha_2-\alpha_1)}\left[e^{-\alpha_1 t}-e^{-\alpha_2 t}\right]\right) = 0 \tag{D.29}$$

Performing the differentiation and simplifying results in

$$\alpha_1 e^{-\alpha_1 t} = \alpha_2 e^{-\alpha_2 t} \tag{D.30}$$

Eq. (D.30) can be simplified further by taking the natural logarithm of both sides as follows

$$\ln\alpha_1 - \alpha_1 t = \ln\alpha_2 - \alpha_2 t \tag{D.31}$$

The time at which V_{peak} occurs, t_{max}, can be determined by solving Eq. (D.31) for t as follows

$$t_{max} = \frac{\ln(\alpha_2/\alpha_1)}{\alpha_2-\alpha_1} \tag{D.32}$$

To determine V_{peak}, Eq. (D.32) is substituted into Eq. (D.13) as follows

$$V_{peak} = v(t_{max}) = \frac{V_{dc}}{R_1C_2(\alpha_2-\alpha_1)}\left[e^{-\alpha_1\ln(\alpha_2/\alpha_1)/(\alpha_2-\alpha_1)}-e^{-\alpha_2\ln(\alpha_2/\alpha_1)/(\alpha_2-\alpha_1)}\right] \tag{D.33}$$

which can be written as

$$V_{peak} = \frac{V_{dc}}{R_1 C_2(\alpha_2 - \alpha_1)}\left[e^{-\ln(\alpha_2/\alpha_1)^{\alpha_1/(\alpha_2-\alpha_1)}} - e^{-\ln(\alpha_2/\alpha_1)^{\alpha_2/(\alpha_2-\alpha_1)}}\right] \quad \text{(D.34)}$$

which is simplified to

$$V_{peak} = \frac{V_{dc}}{R_1 C_2(\alpha_2 - \alpha_1)}\left[\left(\frac{\alpha_2}{\alpha_1}\right)^{-\alpha_1/(\alpha_2-\alpha_1)} - \left(\frac{\alpha_2}{\alpha_1}\right)^{-\alpha_2/(\alpha_2-\alpha_1)}\right] \quad \text{(D.35)}$$

The efficiency, η, is determined by substituting Eq. (D.35) into Eq. (D.28) and simplifying as follows

$$\eta = \frac{(\alpha_2/\alpha_1)^{-\alpha_1/(\alpha_2-\alpha_1)} - (\alpha_2/\alpha_1)^{-\alpha_2/(\alpha_2-\alpha_1)}}{R_1 C_2(\alpha_2 - \alpha_1)} \quad \text{(D.36)}$$

D.4 References

[1] Kuffel E., Zaengl W.S., **High Voltage Engineering: Fundamentals**, 1st ed., Oxford: Pergamon Press, 1984

[2] Craggs John Drummond, Meek John Miller, **High Voltage Laboratory Technique**, London: Butterworth Scientific Publications, 1954

Appendix E

TRANSDUCER ANALYSIS

The voltage and current transducer transfer functions are derived. The magnitude and phase of each are plotted in the frequency domain.

E.1 Voltage Transducer

The RC high pass filter used for the voltage channel transducer in the TICMS design is shown in Figure E.1. The transfer function is determined as follows

$$H(j\omega) = \frac{\overline{V_{out}}}{\overline{V_{in}}} = \frac{R_2}{R_1+R_2+1/(j\omega C)} \tag{E.1}$$

where overlined quantities represent RMS phasors. Multiplying both the numerator and denominator of Eq. (E.1) by jωC and simplifying results in

$$H(j\omega) = \frac{j\omega/\omega_2}{j\omega/\omega_{12}+1} \tag{E.2}$$

where

$$\omega_2 = \frac{1}{R_2C},\ \omega_{12} = \frac{1}{(R_1+R_2)C} \tag{E.3}$$

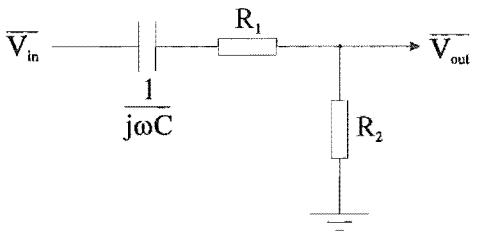


Figure E.1 RC high pass filter

The magnitude response of the voltage transducer in dB is derived from Eq. (E.2) as follows

$$\text{Gain(dB)} = 20\log_{10}\left|\frac{j\omega/\omega_2}{j\omega/\omega_{12}+1}\right| \tag{E.4}$$

which is simplified to

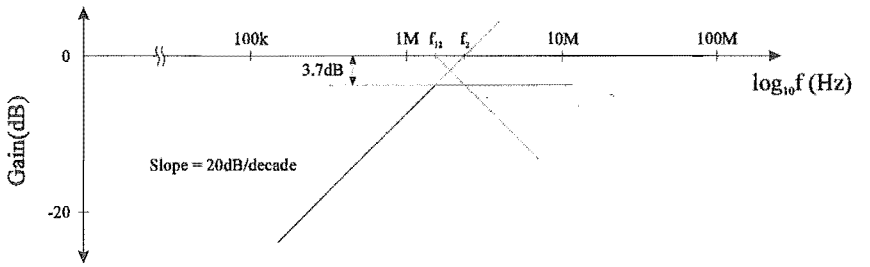
$$\text{Gain(dB)} = 20\log_{10}\frac{\omega}{\omega_2} - 20\log_{10}\sqrt{1+\left(\frac{\omega}{\omega_{12}}\right)^2} \tag{E.5}$$

The phase response is also derived from Eq. (E.2) as follows

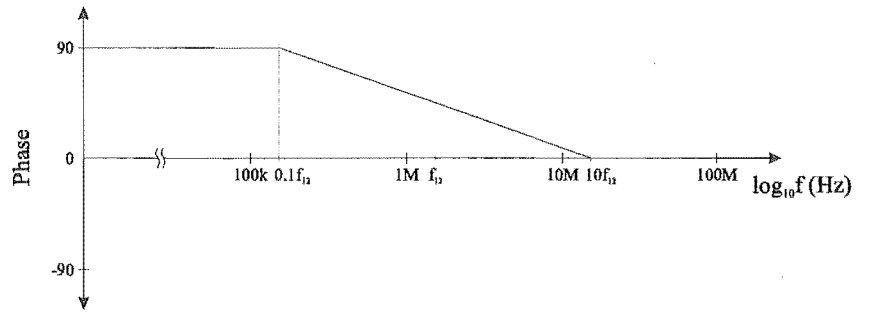
$$\phi = \frac{\pi}{2} - \tan^{-1}\frac{\omega}{\omega_{12}} \tag{E.6}$$

Bode plots of the voltage transducer are obtained by plotting piecewise linear approximations to Eqs. (E.5) and (E.6), as shown in Figure E.2. The attenuation provided by the voltage transducer is calculated as follows

$$\text{Attenuation} = 20\log_{10}\left(\frac{\omega_2}{\omega_{12}}\right) = 20\log_{10}\left(\frac{R_1+R_2}{R_2}\right) \tag{E.7}$$



a)



b)

Figure E.2 Voltage transducer a) magnitude response b) phase response

For the TICMS design R_1 and R_2 are 36Ω and 68Ω respectively, resulting in an attenuation of 3.7dB as indicated in Figure E.2.

E.2 Current Transducer

The RL shunt used for the current channel transducer in the TICMS design is shown in Figure E.3. The transfer function is determined as follows

$$H(j\omega) = \frac{\overline{V_{out}}}{\overline{I_{in}}} = \frac{R_4}{R_3+R_4}\frac{j\omega L(R_3+R_4)}{R_3+R_4+j\omega L} \tag{E.8}$$

which is simplified to

$$H(j\omega) = \frac{j\omega R_4/\omega_c}{1+j\omega/\omega_c} \tag{E.9}$$

where

$$\omega_c = \frac{R_3+R_4}{L} \tag{E.10}$$

The magnitude response of the current transducer in dB is derived from Eq. (E.9) as follows

$$\text{Gain(dB)} = 20\log_{10}\frac{\omega R_4}{\omega_c} - 20\log_{10}\sqrt{1+\left(\frac{\omega}{\omega_c}\right)^2} \tag{E.11}$$

The phase response is also derived from Eq. (E.9) and is equal to

$$\phi = \frac{\pi}{2} - \tan^{-1}\frac{\omega}{\omega_c} \tag{E.12}$$

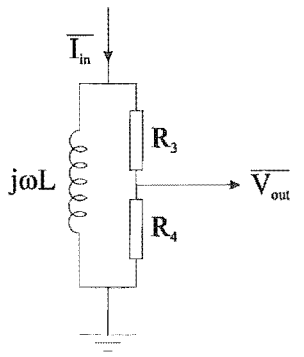


Figure E.3 RL shunt

Bode plots of the current transducer are obtained by plotting piecewise linear approximations to Eqs. (E.11) and (E.12) as shown in Figure E.4.

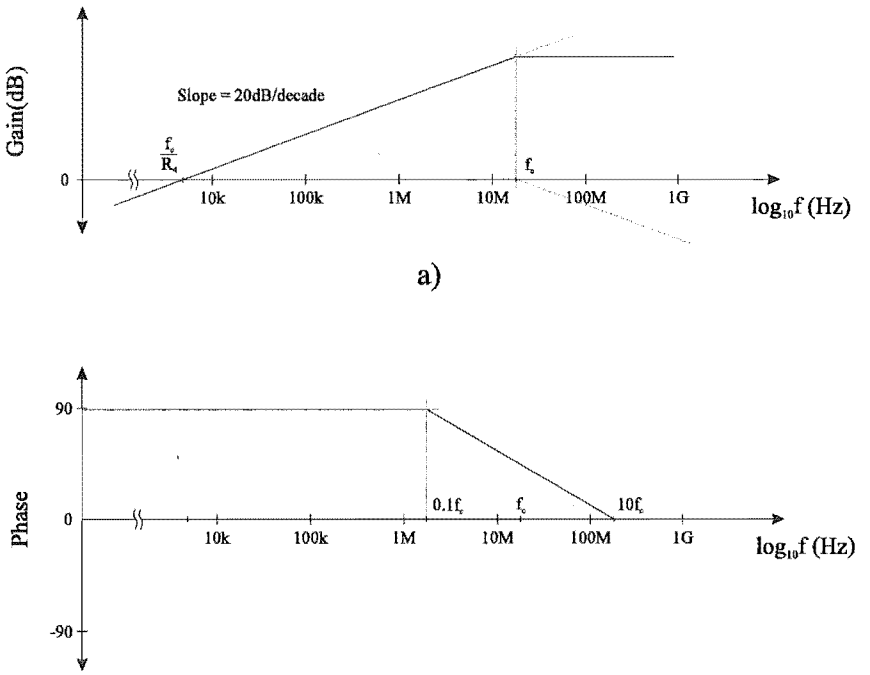


Figure E.4 Current transducer a) magnitude response b) phase response

Appendix F

HEATSINK DESIGN

The current supply requirements of each regulator are presented. This information is then used to calculate the power dissipated in each regulator so that thermal calculations can be made in order to select approriate heatsinks for the regulators.

F.1 DAPM PCB Current Consumption

The DAPM power supply includes four voltage regulators that supply various components in the system. The current supply requirements of each regulator are presented in Table F.1 and Table F.2. The supply requirements of each regulator are worst case values as maximum supply currents are taken from each devices's data sheet. It should be noted that when multiple devices are indicated the supply current given is that for all devices.

Components	+5V Analog	-5.2V Analog	+5V Sampling
LM308(x6)	2.4mA	2.4mA	
OPA642(x4)	58mA	58mA	
LM311	7.5mA	5mA	
ADS605(x2)	200mA	440mA	
30MHz Osc. Module			50mA
74ACT74			5mA*
74ACT02			5mA*
TOTALS	**267.9mA**	**505.4mA**	**60mA**

* Very approximate

Table F.1 Current supply requirements of analog and sampling clock voltage regulators

Component	+5V Digital	Component	+5V Digital
74ACT7811-25(x2)	40mA*	74F11	6.4mA
XC3130A-3	372mA*	74HCT14	5mA
XC1736D	10mA**	32MHz Osc. Module	50mA
TMS320C31	325mA	NS16550AF	160mA
M628128(x4)	520mA	MAX232	75mA
M27C512	30mA**		
		TOTAL	1593.4mA

* Very approximate ** Much less in standby mode

Table F.2 Supply current requirements of digital voltage regulator

F.2 Power Dissipation

The power dissipated in each regulator can be calculated as follows

$$P_{diss} = I_{out} \times (V_{in} - V_{out}) \qquad (F.1)$$

where I_{out} is the current supplied by the regulator from the tables above and V_{in}-V_{out} represents the dropout voltage, the minimum difference between the input and output voltages below which the regulator will cease to function properly. Using Eq. (F.1) the power dissipated in each regulator is calculated and the results are presented in Table F.3. As shown in Table F.3 the positive and negative voltage regulators used have worst case dropout voltages of 2.5V and 3V respectively. A 0.5V margin of safety was added to these values for the P_{diss} calculations.

The power dissipation for each of the main components on the DAPM PCB is given in Table F.4. Using this data the total board dissiptaion is calculated to be 22.5W. To prevent

Regulator	Worst case $(V_{in}-V_{out})^*$ + 0.5V	P_{diss}**
+5V Analog	3V	0.80W
-5.2V Analog	3.5V	1.77W
+5V Sampling	3V	0.18W
+5V Digital	3V	4.78W

* From device data sheets ** Rounded to rwo decimal places

Table F.3 Regulator power dissipation

Component	Power Dissipation	Component	Power Dissipation
Regulators	7.53W	XC1736D	5mW
LM308(x6)	120mW*	TMS320C31	3.15W***
OPA642(x4)	580mW	M628128(x4)	4W
LM311	62.5mW	M27C512	5mW**
ADS605(x2)	3.4W	74F11	32mW
30MHz Osc. Module	250mW	74HCT14	40mW*
74ACT74	40mW	32MHz Osc. Module	250mW
74ACT02	40mW	NS16550AF	800mW
74ACT7811-25(x2)	200mW	MAX232	375mW
XC3130A-3	1.6W		
		TOTAL	**22.5W**

* Very approximate ** When in standby mode

*** Under worst case test conditions

Table F.4 DAPM component power dissipation

the inside temperature of the DAPM enclosure from rising too high a fan and vent are used for cooling. Limiting the local environmental temperature is important if regulator heatsinks are to be as effective as designed.

F.3 Heatsink Design

Thermal resistance is defined as follows

$$R_{\Theta} = \frac{\Delta T}{P_d} \tag{F.2}$$

where R_{Θ}, ΔT and P_d represent thermal resistance, temperature difference and power dissipated respectively. Eq. (F.2) is analogous to Ohm's law and leads to the thermal equivalent circuit for a voltage regulator shown in Figure F.1. An MC78T05CT is used for the +5V analog, +5V sampling and +5V digital voltage regulators. The MC78T05CT can operate at a maximum junction temperature of 150°C. When operated at 120°C the power that can be dissipated is calculated as follows

$$P_d = \frac{120°C - 40°C}{65°C/W} = 1.23W \tag{F.3}$$

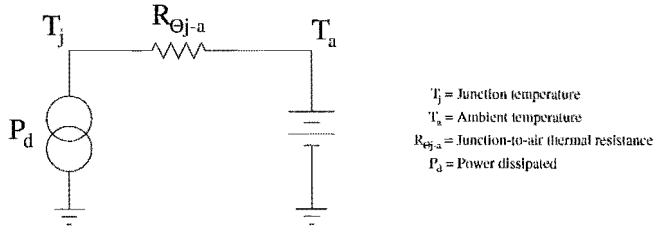


Figure F.1 Voltage regulator thermal equivalent circuit

where $R_{\Theta j-a}$ is 65°C/W from the MC78T05CT data sheet and the internal temperature of the DAPM enclosure is taken to be 40°C. Table F.3 shows that only the +5V digital regulator dissipates more power than that given by Eq. (F.3) and therefore requires a heatsink to prevent the junction from overheating.

The thermal equivalent circuit of the MC78T05CT with a heatsink added is shown in Figure F.2. The junction-to-air thermal resistance needed to keep the maximum junction temperature at 120°C can be calculated as follows

$$R_{\Theta j-a} = \frac{120°C - 40°C}{4.8W} = 16.67°C/W \tag{F.4}$$

From Fig ? $R_{\Theta j-a}$ can be determined as follows

$$R_{\Theta j-a} = R_{\Theta j-c} + \frac{R_{\Theta c-a}(R_{\Theta c-s}+R_{\Theta s-a})}{R_{\Theta c-a}+R_{\Theta c-s}+R_{\Theta s-a}} \tag{F.5}$$

Because $R_{\Theta c-a}$ is much larger than $R_{\Theta c-s}+R_{\Theta s-a}$ then Eq. (F.5) can be approximated as follows

$$R_{\Theta j-a} \approx R_{\Theta j-c}+R_{\Theta c-s}+R_{\Theta s-a} \tag{F.6}$$

By rearranging Eq. (F.6) the maximum thermal resistance of the heatsink can be calculated as follows

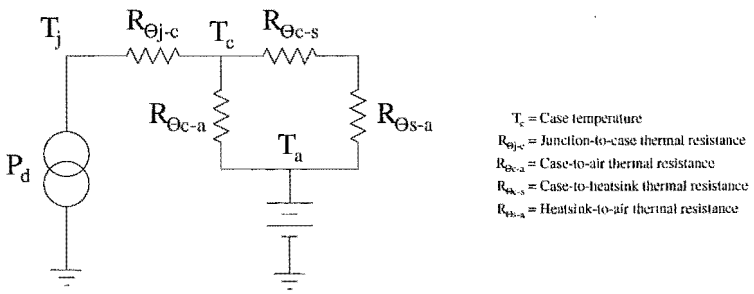


Figure F.2 Voltage regulator and heatsink thermal equivalent circuit

$$R_{\Theta s-a} = 16.67 - 2.5 - 0.5 = 13.67°C/W \quad (F.7)$$

where $R_{\Theta j-c}$ is 2.5°C/W from the regulator data sheet and $R_{\Theta c-s}$ is taken as 0.5°C/W as heatsink paste is used between the regulator and the heatsink [1]. A heatsink with $R_{\Theta s-a}$ equal to 13°C/W is used which keeps the maximum junction temperature just below 120°C.

An LM337T is used for the -5.2V analog regulator. As shown in Table F.3 this regulator dissipates 1.77W and therefore requires a heatsink. The LM337T has a maximum junction temperature of 125°C. When operated at 100°C the $R_{\Theta j-a}$ required to dissipate 1.77W is

$$R_{\Theta j-a} = \frac{100°C - 40°C}{1.77W} = 33.9°C/W \quad (F.8)$$

For the LM337T $R_{\Theta j-c}$ equals 4°C/W. Performing the same calculation as in Eq. (F.7) results in a required $R_{\Theta s-a}$ of 29.4°C/W. A heatsink with $R_{\Theta s-a}$ equal to 28°C/W is used which easily satisfies the thermal requirements.

F.4 References

[1] Williams B.W., **Power Electronics: Devices, Drivers, Applications and Passive Components**, 2nd ed., New York: McGraw-Hill, 1992

Appendix G

TRANSFORMER PHOTOS

Tx_2 was disassembled so that artificial faults could be added. Photographs taken during the disassembly and fault construction process are shown.

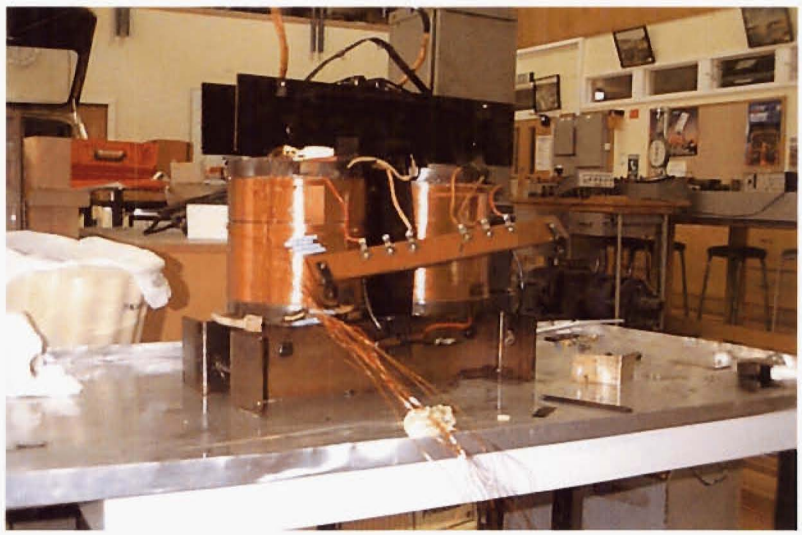


Figure G.1 Front view of tap wires coming from $c_{pri}1$ taken with flash

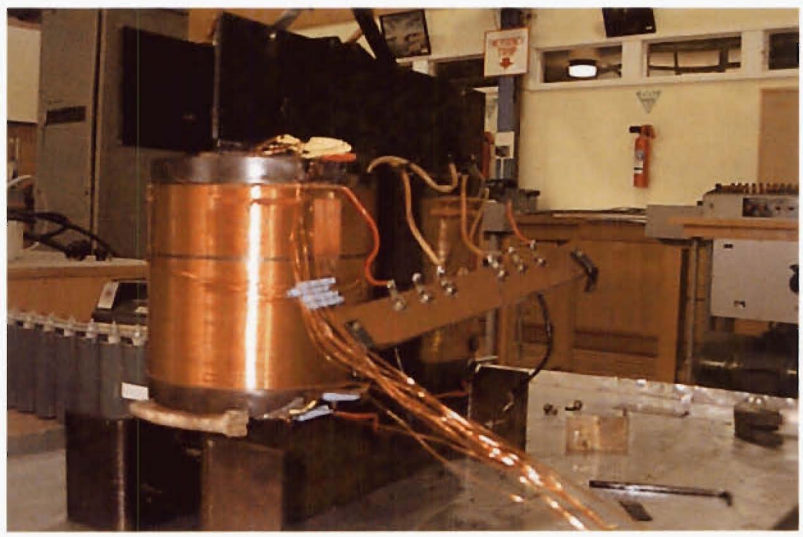


Figure G.2 Side view of tap wires coming from $c_{pri}1$ taken with flash

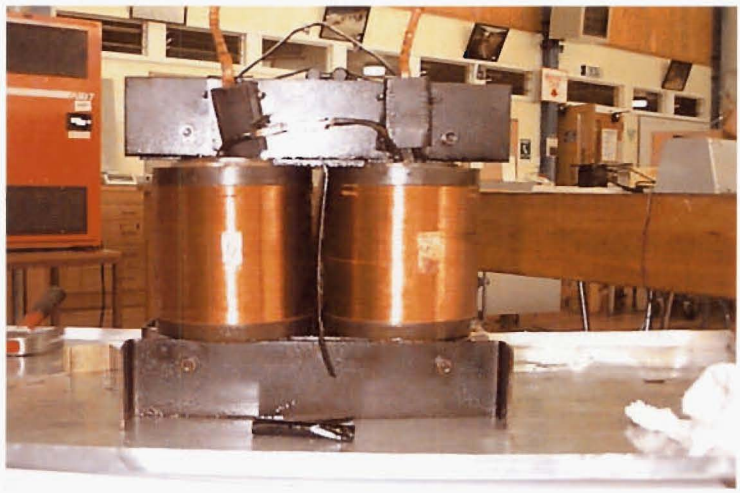


Figure G.3 Back views of $c_{pri}1$ and $c_{pri}2$ taken with flash

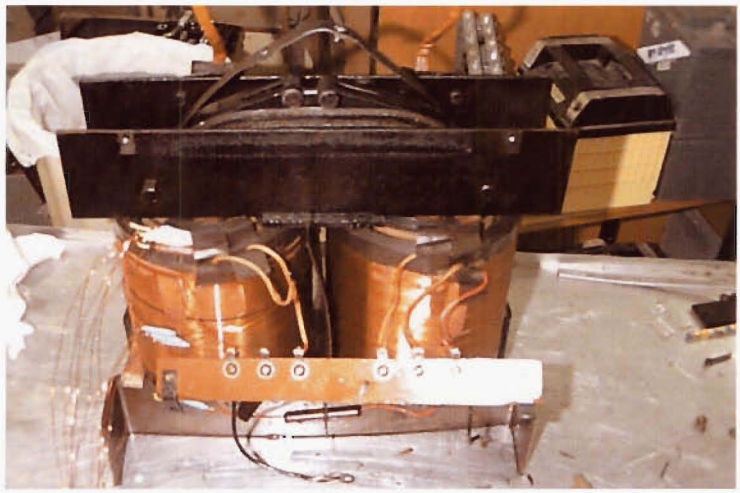


Figure G.4 Top view of $c_{pri}1$ and $c_{pri}2$ taken with flash

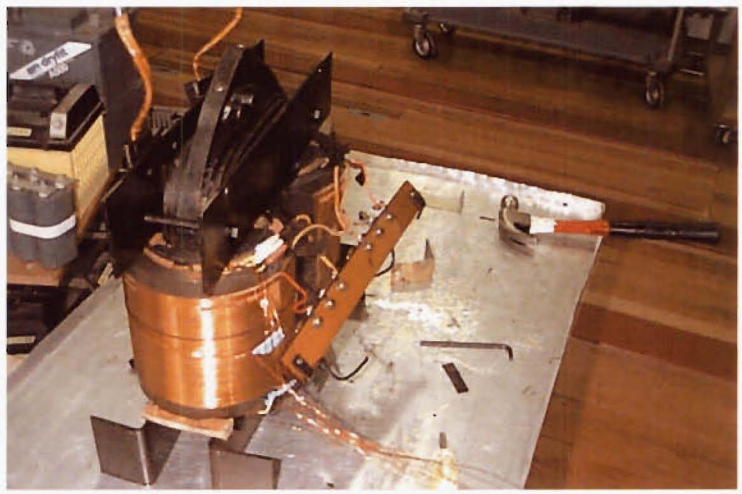


Figure G.5 M1, M2, M3, and M4 tap points visible on outer layer of $c_{pri}1$

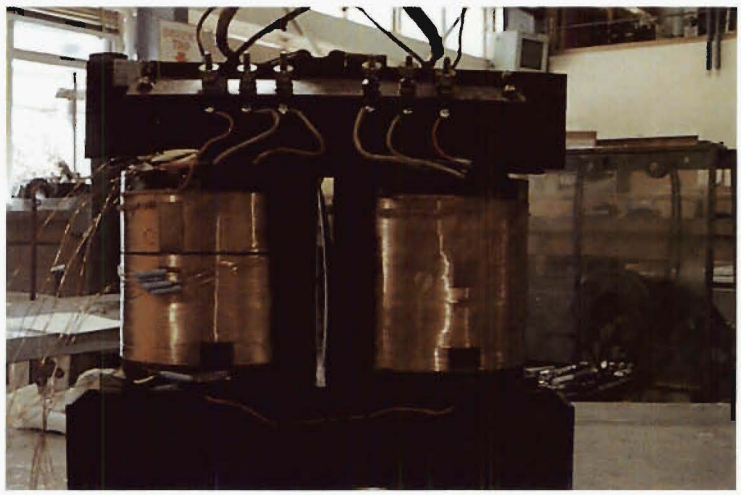


Figure G.6 Tap wires coming off $c_{pri}1$ taken with no flash

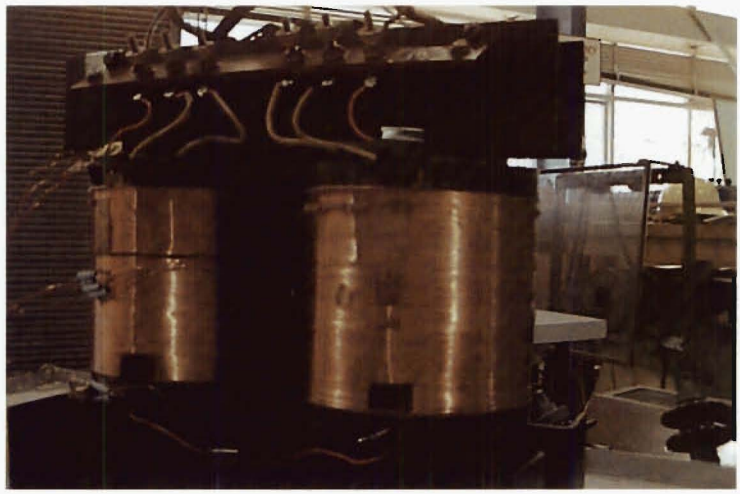


Figure G.7 No flash

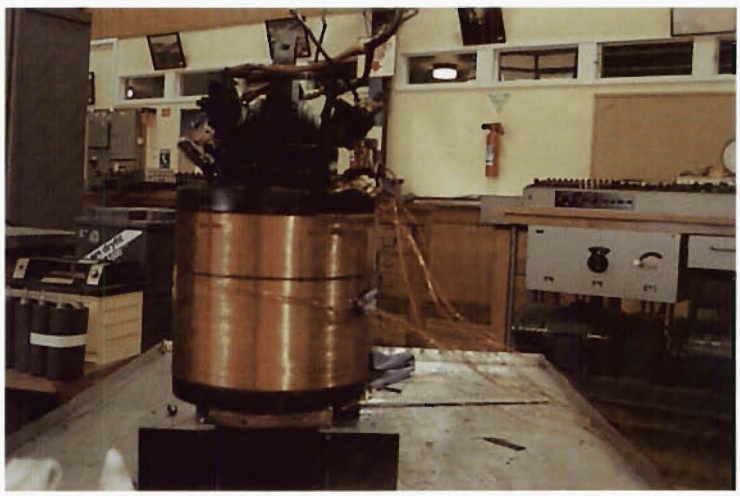


Figure G.8 No flash

Appendix H

PUBLISHED PAPERS

The following two papers by the author have been accepted for publication in *IEEE Transactions on Power Delivery*

1. A Transfomer Insulation Condition Monitoring System
2. The Application of Signal Processing Techniques to Determine a Wideband Transadmittance Function of a Power Transformer Winding

A copy of each paper follows.

Appendix I

TICMS EQUIPMENT PHOTOS

Color photographs showing the TICMS equipment that has been designed and described are presented. Photographs are included that show the online test setup, DAPM, IGM and transformers being tested.

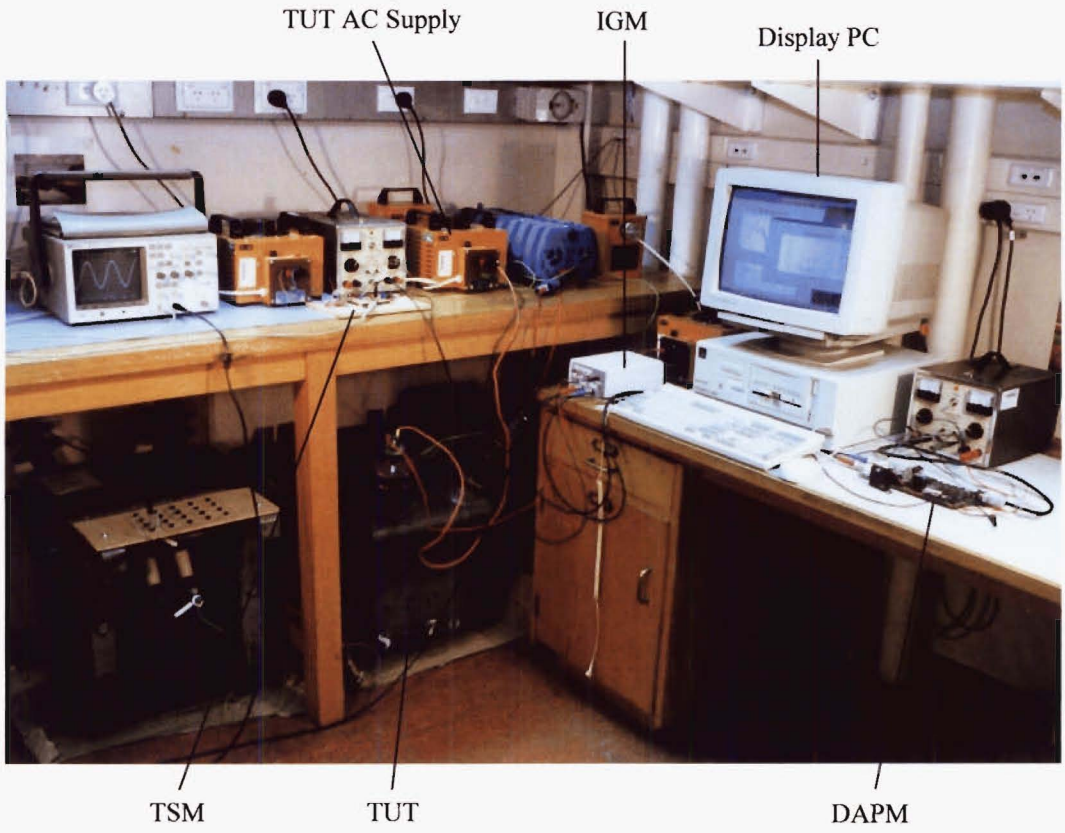


Figure I-1 Online test setup

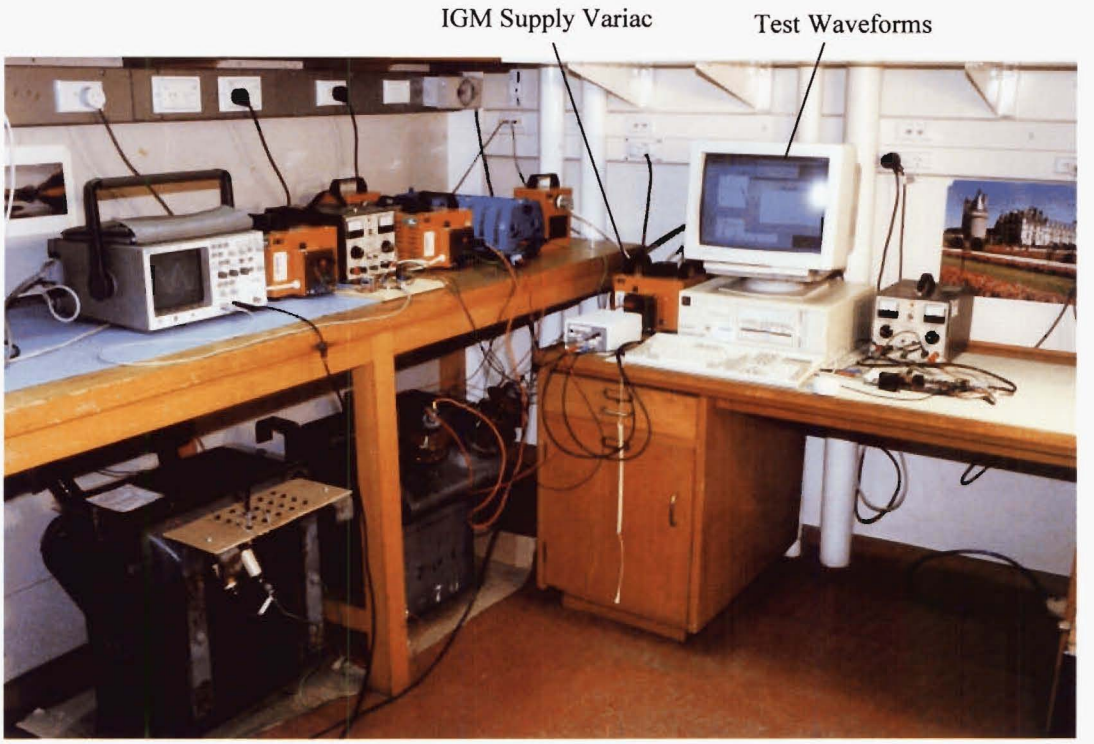


Figure I-2 Online test setup

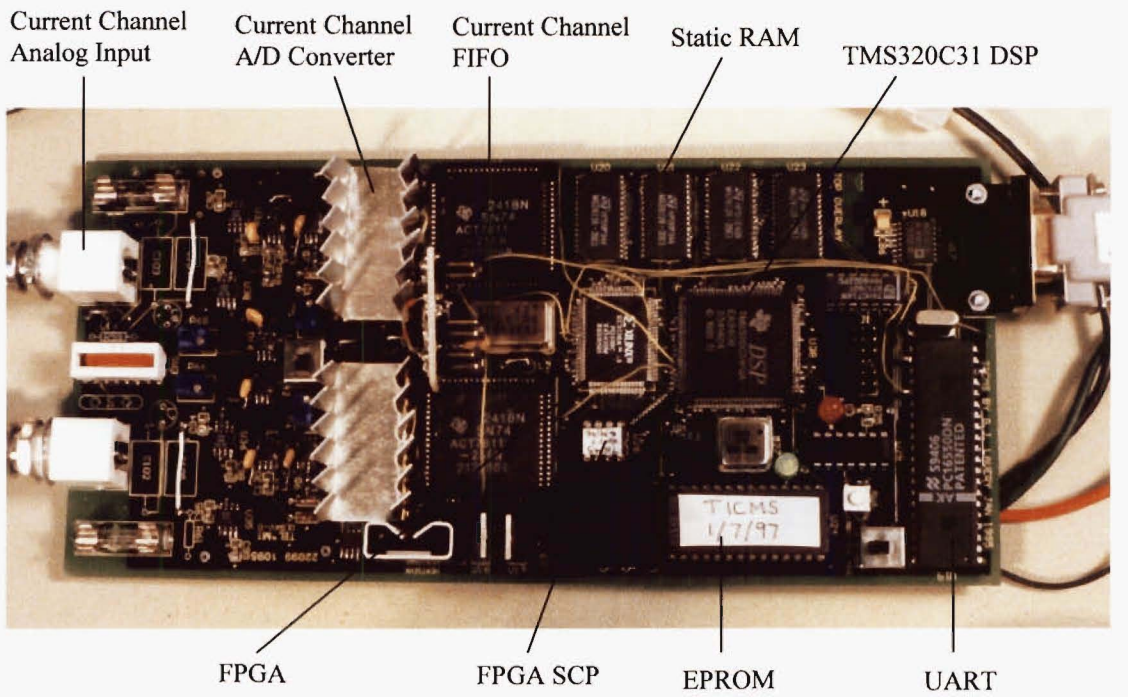


Figure I-3 DAPM

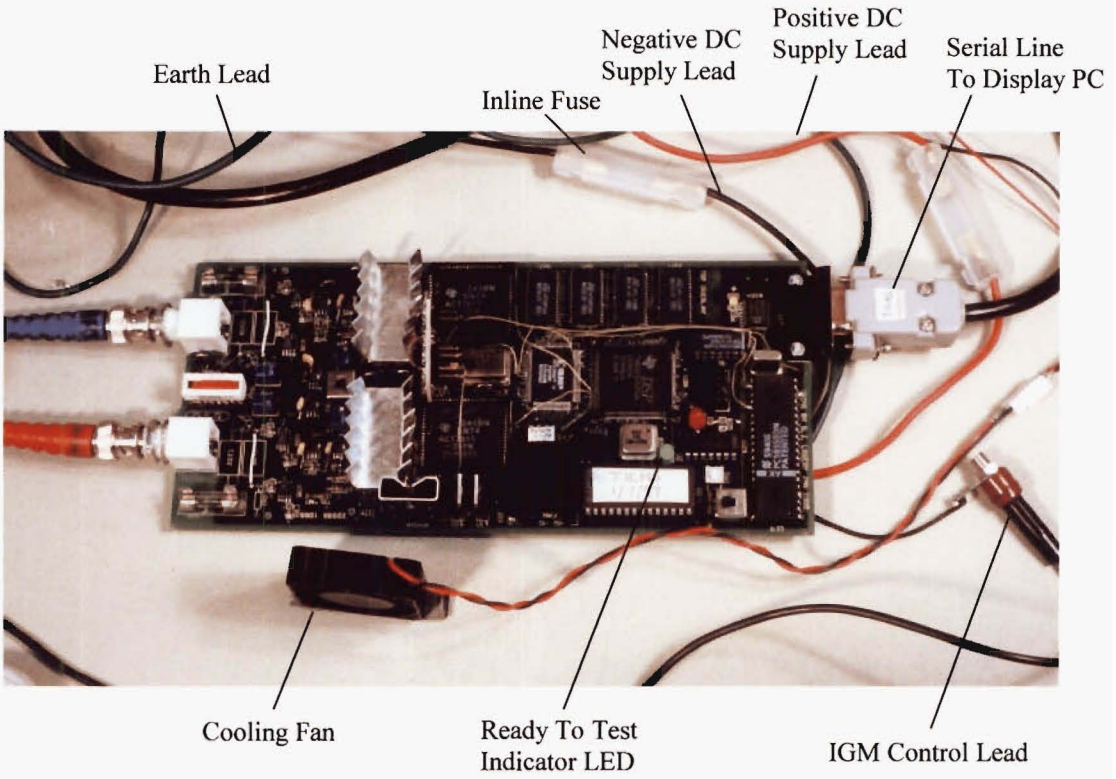


Figure I-4 DAPM

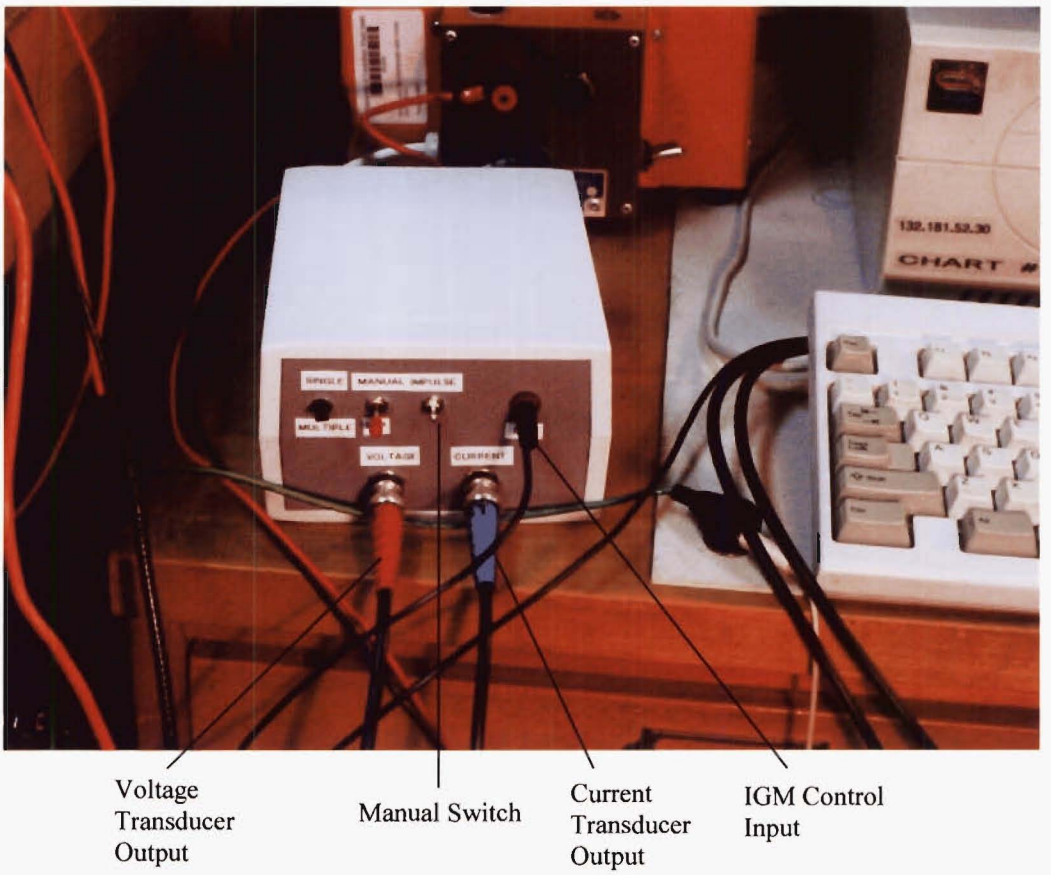


Figure I-5 Current magnitude display window

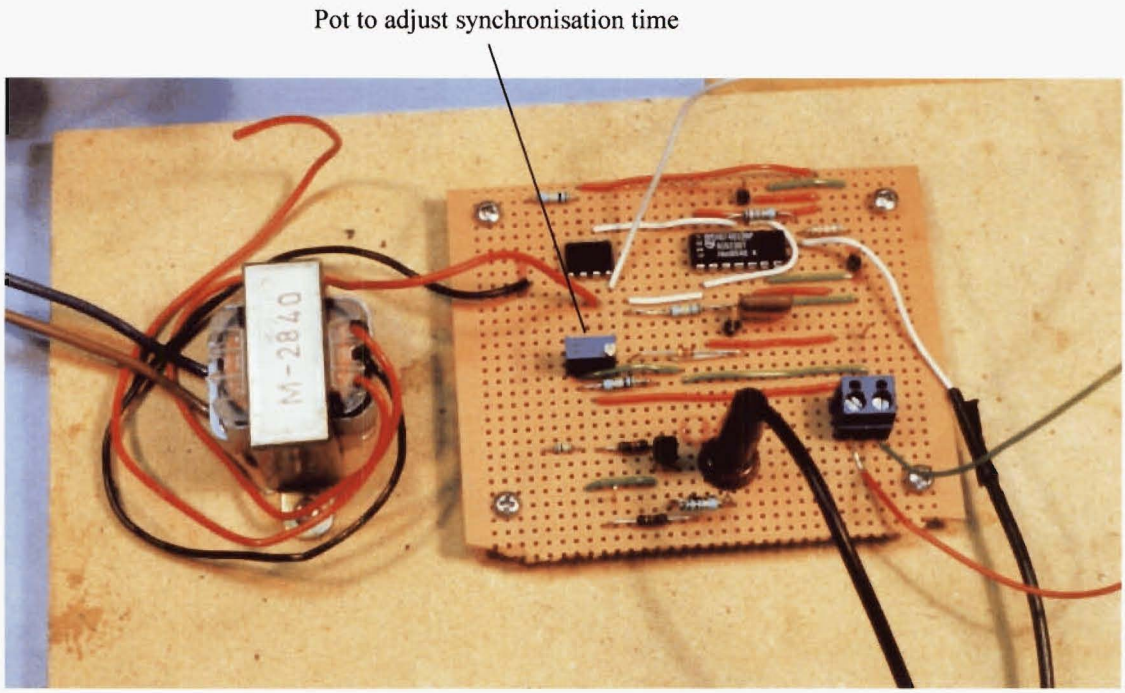


Figure I-6 TSM

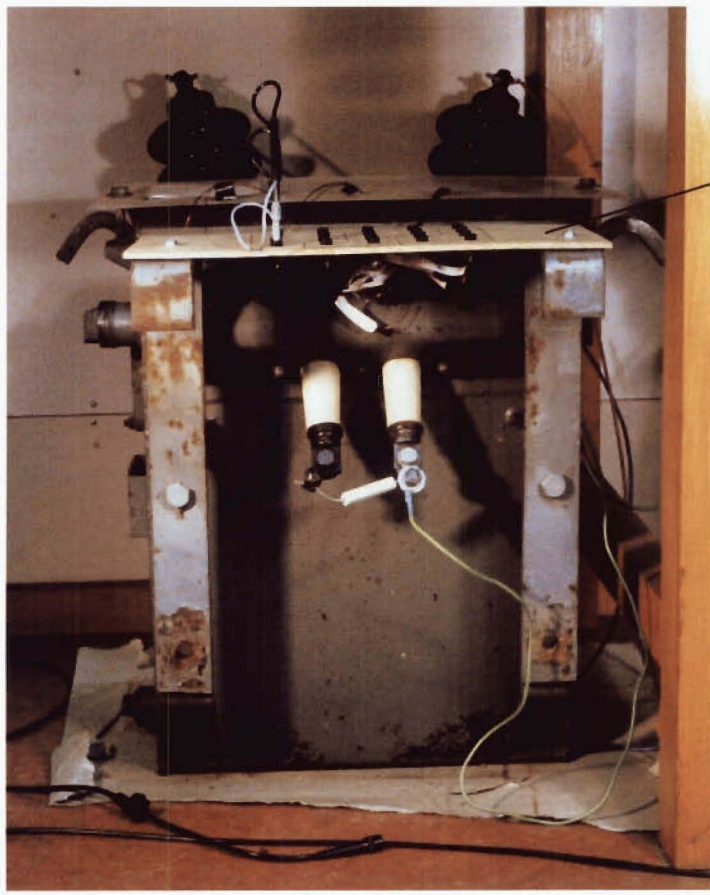


Figure I-7 Transformer Tx2

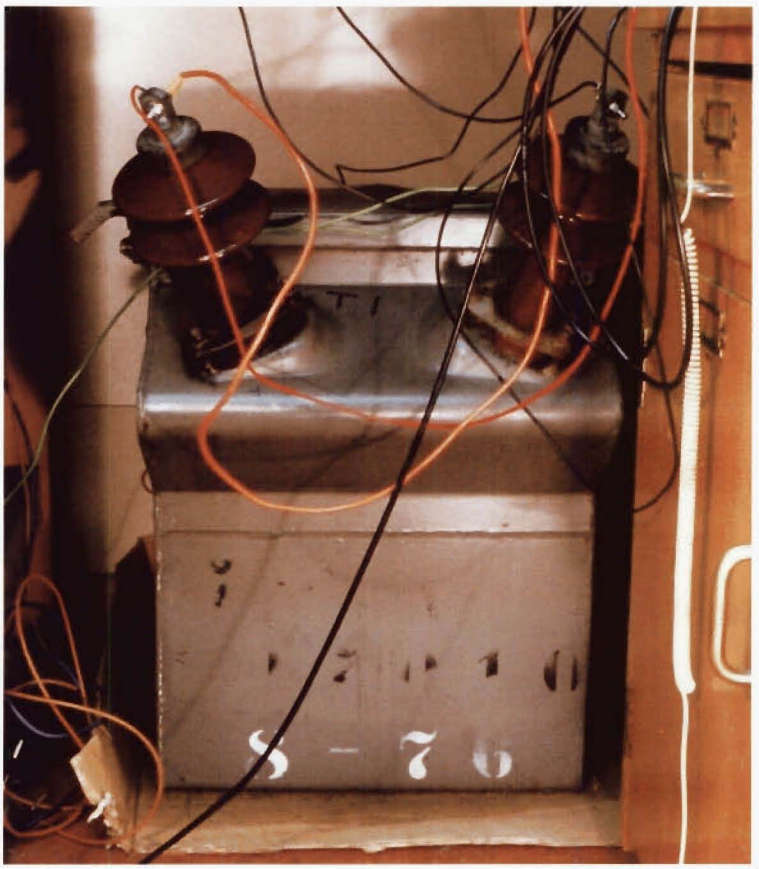


Figure I-8 Transformer Tx1

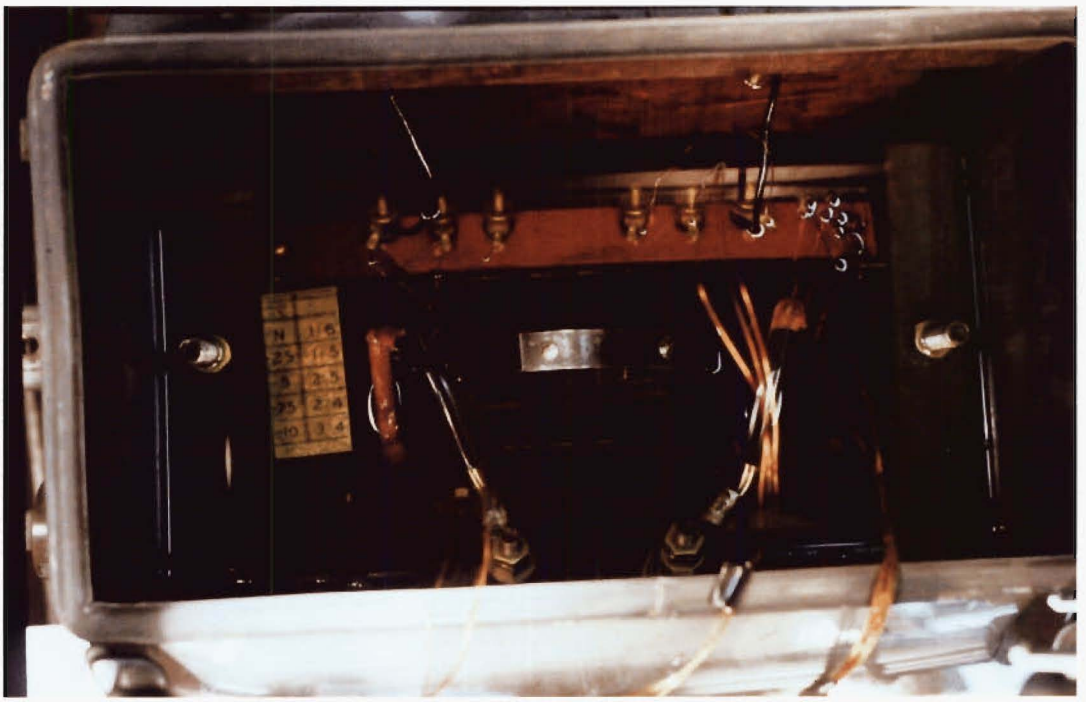


Figure I-9 Inside Tx2

A Transformer Insulation Condition Monitoring System

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Abstract - **A data acquisition and processing system that has been designed to determine the transadmittance function of a power transformer winding in order to evaluate the insulation condition is presented. The key design features of the Transformer Insulation Condition Monitoring System (TICMS) which provide it with the ability to determine the transadmittance function over a 2.5MHz bandwidth in real-time are described. These features include the application of an excitation with tailored spectral characteristics, an analog high pass filter that is used to extend the effective dynamic range of the digitizer, an RL shunt used for transient current measurement, a first-in-first-out (FIFO) memory arrangement that allows the high speed data acquisition section to easily interface to the data processing section and a powerful 32-bit floating point Digital Signal Processor (DSP) that enables the transadmittance function to be determined in real-time. The graphical user interface to the laboratory version of the system is also presented.**

I. INTRODUCTION

Transformer insulation condition tends to degrade over tens of years. The degradation can be attributed to aging, high operating temperatures, transient voltages etc. At present the most often employed method for determining the insulation condition is to take oil samples from the tank at periodic intervals. These oil samples are then taken off for analysis in order to determine what dissolved constituents are present as this gives an indication of insulation condition. On the basis of the results of these tests the transformer may be taken out of service for maintenance.

Because oil sampling only happens on a periodic basis e.g. a well setup system may take oil samples every 6 weeks, then often insulation condition degradation can be missed. Furthermore, depending on whether the transformer has been in service immediately prior to the oil samples being taken or not, the actual oil samples taken may not give a true picture of the state of the oil throughout the transformer tank (i.e. it may give misleading information on the state of the insulation). Consequently there have been a large number of power transformer failures, especially on EHV systems.

The Transformer Insulation Condition Monitoring System (TICMS) is a high speed data acquisition and processing system that has been designed to evaluate insulation condition in real-time by determining the transadmittance function of the winding under test. Here the transadmittance function is defined to be the ratio of the output current response to the input voltage excitation in the frequency domain. Furthermore the TICMS has been designed to determine the transadmittance function up to 2.5-3MHz [1] which in principle enables breakdown between individual turns in certain winding types to be detected [2]. Existing systems surveyed by the authors determine the transadmittance function to around 1-1.5MHz which only allows interdisc breakdown to be detected in power transformers.

At present the TICMS is being used for off-line testing in a laboratory setup. However ultimately the research is aimed at using the system for on-line testing so that degradation can be detected in real-time and action taken to remove a faulty transformer from service before failure takes place. On-line testing will also enable transformers to be run to the maximum of their operating life before maintenance needs to be carried out i.e. much more efficient and cost effective maintenance schedules can be applied.

II. TRANSFORMER WINDINGS

A transformer in general possesses a limited number of major resonances which are determined by the winding construction. Three main types of winding are used in transformers, namely disc, interleaved disc, and layer. Disc and sometimes interleaved disc windings are used for the primary winding of EHV transformers. Over a frequency

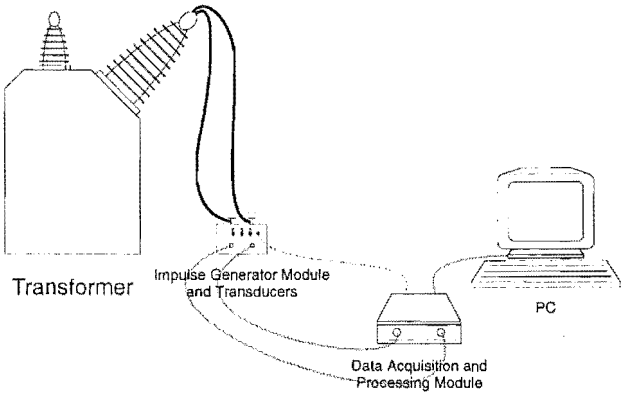

Fig. 1. The Transformer Insulation Condition Monitoring System

range of 20kHz to 1.2MHz, disc windings have a dominant pole around 0.5-0.6MHz, interleaved disc have a few major poles between 0.3 and 0.8MHz while layer windings show a number of overlapping adjacent poles [5-6]. A 7.5kVA 11kV/230V distribution transformer with a layered winding construction has been tested using the TICMS. The resulting transadmittance function is illustrated in Fig. 6. The TICMS has been effective in detecting artificial faults in this transformer, as discussed in IV. It is expected that the pole location for disc and interleaved disc windings will allow the TICMS to detect faults in these winding types.

III. DESIGN FEATURES OF THE TICMS

The TICMS consists of two instruments and an attached PC and is connected to a transformer as shown in Fig. 1. The first instrument is a low voltage Impulse Generator Module (IGM) that provides the excitation needed to determine the transadmittance function. The second instrument is a high speed Data Acquisition and Processing Module (DAPM) that digitizes the impulse along with the response from the transformer so that digital signal processing can be used to determine the winding transadmittance function. This is then interpreted to evaluate winding insulation condition.

Transducer circuitry is used to interface the system to the transformer and to attenuate the signals down to a level compatible with the DAPM. The transducer circuitry is

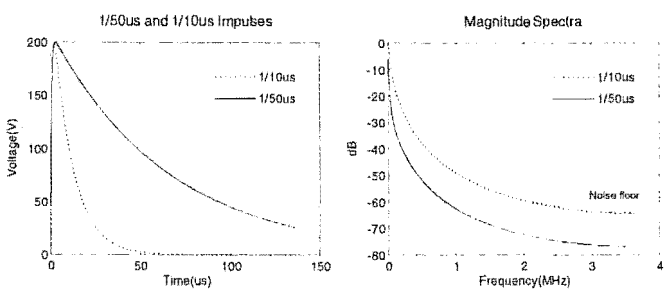

Fig. 2. Impulses in the time and frequency domains

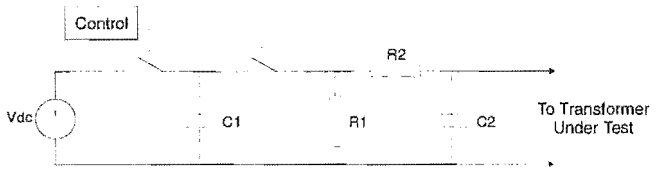

Fig. 3. Impulse generator

housed in the IGM enclosure.

A high speed serial link is used to attach the DAPM to the PC. The PC is used to issue commands to the DAPM and receives captured and processed data in response. A custom designed Windows95 application then displays this data graphically for user interpretation. A control line between the DAPM and the IGM allows test procedures to be automated.

A. *Impulse Generator Module*

The IGM consists of a single stage impulse generator circuit and control circuitry. A simplified representation of the impulse generator circuit is shown in Fig. 3. The RC values are used to control the waveshape of the impulse. The TICMS uses a 1/10μs waveshape as opposed to the standard 1.2/50μs waveshape that is often used for transformer impulse testing as the former has high frequency components that are larger in magnitude than the corresponding components of the longer tailed impulse. Thus the use of the shorter tailed impulse allows the transadmittance function to be determined to a higher frequency as the magnitude spectrum drops below the quantization noise floor imposed by the analog-to-digital conversion process at a higher frequency as shown in Fig. 2 [1]. The control circuitry is responsible for opening and closing the switches in Fig. 3 at the correct times. A control input from the DAPM can activate the control circuitry allowing an insulation test to be initiated through software.

Rectified mains supplied via a variac is used as the source of DC in Fig. 3 which allows the user to control the peak voltage of the impulse produced. The IGM is capable of generating an impulse with a maximum peak voltage of 200V when the variac is on full.

B. *Transducers*

To get the voltage impulse in a form suitable for digitization the TICMS uses an analog high pass filter as shown in Fig. 4. When the filtered impulse occupies the full-scale input voltage range of the digitizer then the frequency at which its magnitude spectrum drops below the noise floor is increased relative to that of the unfiltered impulse. This allows the transadmittance function to be determined to a higher frequency [1]. The lower frequencies that are attenuated by the filter are recovered by digitally dividing the spectrum of the filtered impulse by the transfer function of the high pass filter thus ensuring that the transadmittance function

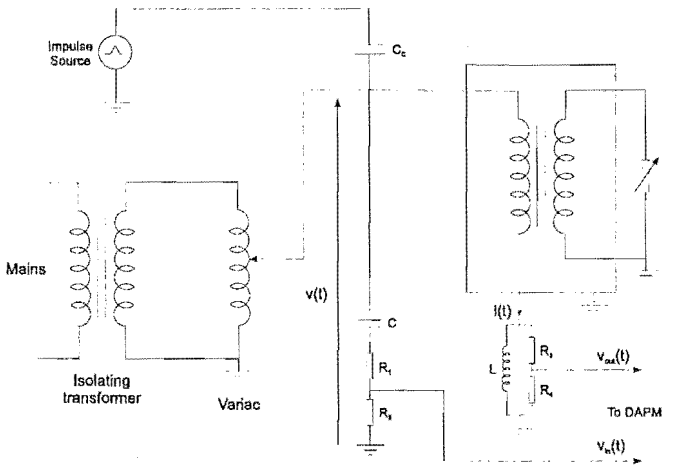

Fig. 4. Voltage and current transducers

can still be determined at low frequencies [1]. In summary the filtering operation increases the effective dynamic range of the voltage channel.

The voltage drop across an RL shunt is used to measure the current response as shown in Fig. 4. The shunt is designed so that its reactance is low at low frequencies and high at high frequencies. Consequently it has a similar effect to the high pass filtering operation discussed above, namely in increasing the frequency at which the magnitude spectrum of the current response drops below the noise floor as the large magnitude low frequency components that occupy most of the dynamic range are attenuated. Furthermore the RL shunt can be designed to have negligible reactance at 50Hz which allows it to be used for current measurement in an on-line situation.

The output signals from the RC filter and the RL shunt are buffered prior to being connected to the DAPM with 50Ω coax. The coax is terminated with 50Ω so that voltage reflections don't take place over the frequency range of interest should the coax cable length be increased.

C. *Data Acquisition and Processing Module*

The DAPM digitizes the analog signals from the RC filter and RL shunt in Fig. 4 so that digital signal processing can be used to determine the transadmittance function. The DAPM is depicted in Fig. 5.

1) Analog Signal Processing

Before the analog signals can be digitized some analog signal conditioning is needed to get them into a form suitable for digitization. As already discussed an RC filter and RL shunt are used to attenuate the large magnitude low frequency components, increasing the effective dynamic range of the system so that the transadmittance function bandwidth can be increased as needed. Resistive voltage dividers are used to accurately control the amplitude of the transient signals as shown in Fig. 4. This ensures that the filtered signals occupy the full-scale input voltage range of the analog-to-digital converters thus maximizing the signal-to-noise ratio during digitization.

In order to make sure that the output signal from the RC filter is not too small in amplitude and requiring that amplification be used, the RC filter is attached directly to the transformer so that the voltage impulse is filtered before any attenuation takes place.

Because the waveshape of the excitation is controllable then low pass anti-aliasing filters are not used prior to digitization as the spectral characteristics of the analog signals are known in advance. The absence of anti-aliasing filters mean that a lower sampling rate can be used as the filter transition band does not need to be accounted for. This results in less data being generated and enables the TMS320C31 DSP used to determine the transadmittance function in real-time.

2) Analog-to-Digital Conversion

The frequencies at which the magnitude spectra of the analog inputs drop below the quantization noise floor determines the minimum sampling rate that can be used on each channel if aliasing is to be avoided [1]. The RC filter and RL shunt in Fig. 4 are designed to enable the transadmittance function to be determined to 2.5-3MHz which requires that a sampling rate of at least 6MHz be used. Each channel uses an analog-to-digital converter that samples at 10MHz with 12-bits of vertical resolution. A sampling rate of 10MHz is used as it is possible to obtain frequencies above 3MHz that are above the noise floor for the current response due to transformer resonances.

3) FIFO Rate Buffers

A sampling rate of 10MHz requires that rate buffers be

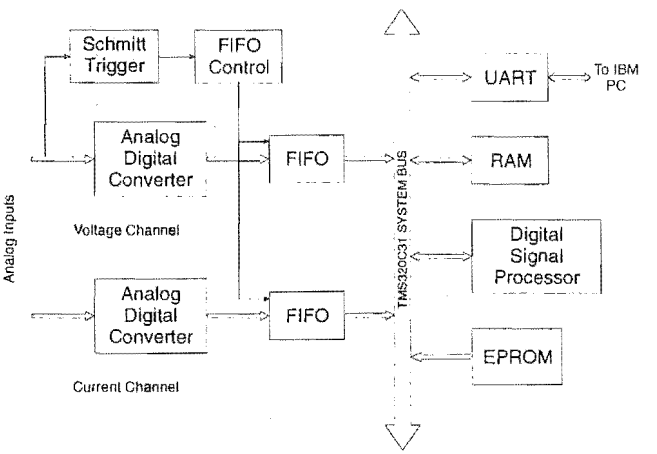

Fig. 5. Data acquisition and processing system

used between the converters and the DSP as the I/O data transfer rate of the DSP is not high enough to receive the sampled data directly. High speed first-in-first-out (FIFO) memories are used to implement the rate buffers as shown in Fig. 5. Each FIFO is capable of holding 1024 samples when full. For a sampling rate of 10MHz this represents a total time record of 102.4μs which is more than enough to capture the filtered voltage and current transients for the 7.5kVA 11kV/230V transformer tested.

As future test setups may require the digitization of a transients that exceed 102.4μs, the DSP's on chip direct memory access (DMA) controller can be used to transfer data from the current FIFO to the DSP's internal RAM while the converter writes samples to the FIFO. The DMA data transfer rate is 5.56Msamples/s and as samples arrive from the converter at 10Msamples/s then current FIFO fills at 4.44Msamples/s. The DMA transfer starts when the FIFO contains 64 samples so that it takes 216μs for the remaining locations to fill. In this time up to 1200 samples can be transferred, easily allowing a total of 2048 samples to be recorded for the fast Fourier transform (FFT) algorithm. Without the use of DMA to increase the effective rate buffer size the analog transients may be truncated which would then require the use of additional digital signal processing to window the data and may result in errors being introduced.

The dual port nature of the FIFOs also enables the TICMS to continuously sample the analog inputs when a test is not in progress, retaining the 32 most recent samples. This ensures that information about the analog signals is not lost before the schmitt trigger in Fig. 5 initiates the transient recording process.

4) Digital Signal Processing

A TMS320C31 32-bit floating point DSP is used to implement the required signal processing operations of the TICMS. These operations include transferring the captured time domain data into the frequency domain using a modified 2048 point decimation-in-time (DIT) FFT algorithm that transfers voltage and current data simultaneously for computational efficiency [1], digitally dividing the magnitude spectrum of the filtered voltage impulse by the transfer function of the high pass filter and the calculation of the transadmittance function magnitude and phase from the spectra of the captured data. The DSP can also improve the frequency resolution of the transadmittance function over a band of interest by frequency shifting, filtering and decimating the time domain data.

After startup the DSP program code is shadowed in zero wait-state external static RAM to increase the execution speed. As 16K of the 128K of RAM has been reserved for program code then 112K is available for data storage. The TICMS can use this memory to store results from up to 112 previous tests depending on how much data per test is stored. This makes it possible to temporarily determine the transadmittance function at a rate that exceeds that determined by the data transfer rate to the PC for the laboratory version of the system.

D. TICMS Display PC

The TICMS uses a Universal Asynchronous Receiver Transmitter (UART) to interface to the serial port of the attached PC so that test data can be sent for user interpretation. The data transfer rate of this serial link is 57.6kbits/s although it is capable of 115.2kbits/s if the cable length is short enough. As the frequency domain description of real data is symmetrical then only half of the 32-bit data words needs to be sent. When sending only the transadmittance magnitude the transmission time is 570ms at 57.6kbits/s.

The receiving PC runs a custom designed Windows95 application that displays insulation test data graphically. Data

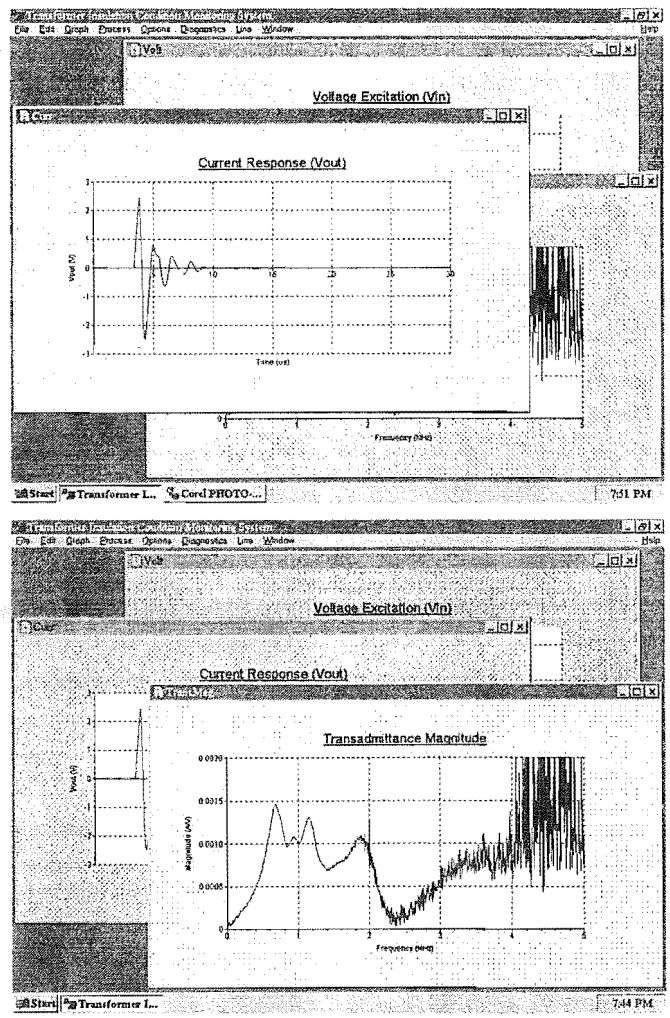

Fig. 6. The TICMS display

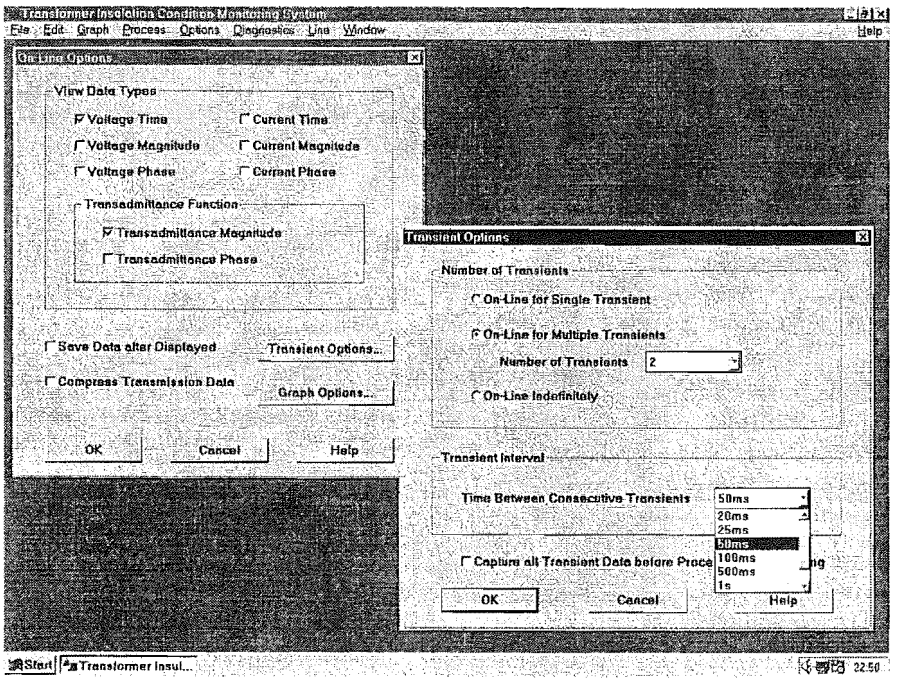

Fig. 7. The TICMS configuration interface

obtained from testing a 7.5kVA 11kV/230V distribution transformer is shown in Fig. 6 where it can be seen that there are poles in the transadmittance function at 700kHz, 950kHz, 1.15MHz and 1.9MHz respectively.

Incoming data is time stamped for future reference and is optionally archived to hard disk. Data is normally archived in a binary file format for storage efficiency but the system also allows the user to save the data as a text file so that it can be imported into MATLAB for postprocessing. This allows future digital signal processing operations to be trialed on real data before committing them to TMS320C31 code.

E. TICMS Control

The attached PC sends a command to control the operation of the TICMS when the system goes on-line. The DSP decodes this command and performs the operations as instructed. For experimental purposes commands are available to control the data sent, the number of consecutive tests to be performed and the time interval between these tests as shown in the configuration interface in Fig. 7. Using these options the user can set up the TICMS so that each time the system goes on-line the transadmittance function is determined either once, a given number of times or indefinitely.

Options are also available that allow the user to control how the incoming data is displayed. This allows either existing graphs to be updated with new data or multiple data sets to be plotted on the same set of axis for ease of comparison.

IV. APPLICATION OF THE DEVICE

Artificial faults have been placed into the winding of a 7.5kVA 11kV/220V distribution transformer. This was accomplished by disassembling the transformer, inserting tap points, and then using links to introduce faults. A number of faults between layers were introduced between the HV end and the middle of the winding. Faults between turns were placed in the outer layer, half way between the middle and the HV end of the winding. In general there is no restriction on where the faults could be placed. The locations used were easily accessible, and did not require having to unwind coils. Changes in the pole characteristics were detected for each fault, and the finding are being presented in a forthcoming paper.

The system has been used to test a 2nd 7.5kVA transformer while energised with a mains supply. This was accomplished using the setup illustrated in Fig. 4. Energising the transformer leads to changes in the self and mutual inductance which contribute the form of the transadmittance function [5]. As a result differences in the on-line transadmittance function were measured. Additional on-line tests have been performed to evaluate the effect of load current, supply amplitude, oil temperature and point in the 50Hz cycle at which the IGM is activated. The effect of each of these parameters on the transadmittance function was evaluated and the results are being reported in a forthcoming publication.

For on-line testing in the field, additional TICMS analog inputs will be used to monitor temperature, transformer tap changer position and load current. DAPM software additions will be made so that the effect of these parameters on the transadmittance function can be distinguished from changes caused by winding insulation faults.

V. CONCLUSIONS

A high speed data acquisition and processing system designed to evaluate power transformer winding insulation condition by determining the transadmittance function has been presented. The system described is the latest to evolve from the research activities of the author over the last 2 years at the University of Canterbury and differs from existing systems in that it enables the transadmittance function to be determined to 2.5-3MHz [1] which in principle allows shorts between individual turns in certain winding types to be detected [2].

A powerful floating point DSP has been used to determine the transadmittance function in real-time as the research is ultimately aimed at using the system to perform on-line testing. This enables the evaluation of the winding insulation condition while the transformer is in service so that a faulty transformer can be taken out of service before failure takes place. On-line testing involves capacitively coupling the low voltage excitation used by the TICMS onto the transformers sinusoidal input while the RL shunt is used to determine the current response as discussed previously. The high pass characteristic of the RC filter and the RL shunt attenuate the large 50Hz component, preventing it from taking up dynamic range so that no additional digital signal processing is needed for on-line testing. Additional front-end hardware development may be needed when testing transformers in service as the instrumentation system will be exposed to high frequency noise from other sources in the power system.

Artificial faults have been placed in the winding of a 7.5kVA 11kV/230V distribution transformer in order to relate particular faults to changes in the transadmittance function, as previously discussed. This information will then allow the system to compare successive transadmittance functions and generate an alarm signal if insulation condition degradation is found to have taken place. Thus the system will eventually become a 'black box' that permanently sits beside a transformer continuously evaluating insulation condition.

VI. ACKNOWLEDGMENTS

The financial assistance of the University of Canterbury Doctoral scholarship for G.J.Lavery is gratefully acknowledged. The authors would also like to thank Southpower for donating transformers for testing.

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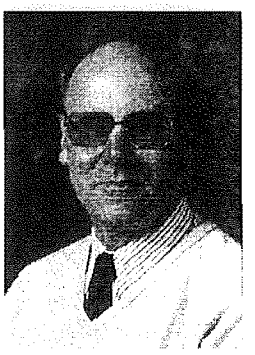
VIII. BIOGRAPHIES

Grant J. Lavery received a BE degree with first class honors in electrical engineering from the University of Canterbury New Zealand in 1993. He is currently pursuing postgraduate research leading to a Ph.D. degree at the University of Canterbury N.Z.



Michael B. Dewe received the B.Sc. degree from the University of Capetown South Africa in 1964, and an ME degree from the University of Canterbury New Zealand in 1966. He worked for the Space Division of Hawken Siddeley Dynamics Ltd (now British Aerospace Ltd), U.K., until 1972 where he was Group Leader of Electronic Systems Design. He was a Senior Lecturer at the University of Witwatersand S.A. until taking up a similar post with the University of Canterbury in 1978. In 1981 he joined Wormald Vigilant Ltd. N.Z., where he was Engineering Manager and Associate Director until rejoining the University of Canterbury in 1985. His prime research interests are in the field of applying state-of-the-art techniques to power system instrumentation.

The Application of Signal Processing Techniques to Determine a Wideband Transadmittance Function of a Power Transformer Winding

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Abstract - **The transadmittance function of a power transformer winding is used to evaluate the insulation condition of the winding. This paper presents the signal processing techniques that are used to determine the transadmittance function as implemented in the Transformer Insulation Condition Monitoring System (TICMS) - a high speed data acquisition and processing system that has been designed to determine the transadmittance function in real-time. The use of an RC high pass filter and an RL shunt to increase the effective dynamic range of the analog-to-digital converters so that the transadmittance function bandwidth can be increased is one of the key features of this system. A radix-2 decimation-in-time (DIT) fast Fourier transform (FFT) algorithm is then introduced that transforms data from the voltage and current channels of the TICMS into the frequency domain simultaneously so that the computational performance of the system is increased. The digital signal processing required to determine the transadmittance function from the transient signals resulting from the RC filter and RL shunt are then introduced. The transadmittance function of a 7.5kVA 11kV/230V distribution transformer is then determined and compared with that obtained by performing a sweep frequency test on the transformer.**

I. INTRODUCTION

The transadmittance function of a power transformer winding can be used to fingerprint the insulation system and thus provide a means of monitoring its condition. The transadmittance function is defined to be the ratio of the output current response to the input voltage excitation in the frequency domain. If the transadmittance function is to be used to detect interturn breakdown then it must be determined over a wide frequency range. For EHV transformers 2.5MHz is generally considered sufficient [2]. Previous attempts have been successful at determining the winding transadmittance function to approximately 1.5MHz which only allow interdisc breakdown to be detected in these transformers [2].

The Transformer Insulation Condition Monitoring System (TICMS) [1] is a high speed data acquisition and processing system that employs a powerful 32-bit floating point Digital Signal Processor (DSP) to determine the transadmittance function in real-time. This paper presents some of the signal processing techniques used by the TICMS to ensure that the transadmittance function can be determined up to a bandwidth of 2.5-3MHz.

The TICMS has been used in a laboratory setup to determine the transadmittance function of a single phase 7.5kVA 11kV/230V distribution transformer. For the layered winding used in this transformer the transadmittance function was found to consist of a series of poles as shown in Fig. 6. Tests are about to start on a 200kVA 11kV/230V unit. Similar tests on a larger rating power transformer are now being scheduled.

II. THE TRANSADMITTANCE FUNCTION

Fig. 1 shows a simplified equivalent circuit representation of a power transformer winding where M_i represents the mutual inductance between two winding elements that are separated by i-1 elements. Such a model has limited application in trying to model the high frequency behavior of the winding due to the decrease in the permeability of the iron core with increasing frequency but is useful for illustrating the transadmittance function concept.

According to linear circuit theory the input and output signals of the 2-port network in Fig. 1 are related according to the convolution equation

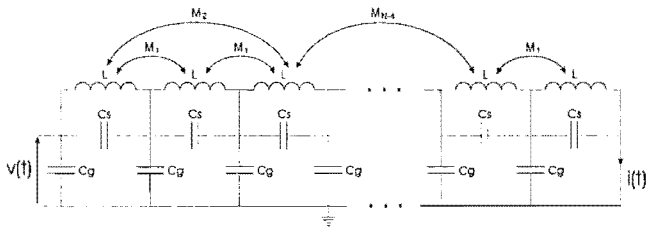

Fig. 1. Simplified winding equivalent circuit

$$i(t) = \int_{-\infty}^{+\infty} v(\tau)h(t-\tau)d\tau \tag{1}$$

where h(t) is the impulse response. The transadmittance function H(f) can be determined by transforming (1) into the frequency domain and rearranging to produce

$$H(f) = \frac{I(f)}{V(f)} \tag{2}$$

The transadmittance function thus characterizes the winding and any changes that take place in the winding insulation condition due to deterioration are reflected as changes in the transadmittance function.

In general the transadmittance function is a complex quantity and its magnitude can be determined by dividing the magnitude of I(f) by that of V(f) while the phase is determined by subtracting the phase of V(f) from that of I(f).

III. DATA ACQUISITION

The TICMS samples the voltage and current analog transient signals that result from an insulation test and uses digital signal processing to determine the transadmittance function. The time domain signals are sampled at 10MHz and as the high frequency components above half the sampling frequency are below the quantization noise floor for both channels then no anti-alias filtering has to be implemented. If anti-aliasing filters had been used then a much higher sampling rate would be needed to account for the filters transition band. This would lead to a large amount of data being generated and as a consequence larger and faster rate buffers would be needed between the analog-to-digital converters and the DSP [1] which would make the design of the system more difficult.

The quantization that takes place during the digitization process causes a random noise component to be added which gives rise to a quantization noise floor in the frequency domain. For an ideal N-bit analog-to-digital converter the Signal-to-Noise ratio (SNR) is

$$SNR = -(6.02N + 1.76)\text{dB} \tag{3}$$

where 0dB represents the magnitude of a sinusoid that takes up the full dynamic range of the converter.

The TICMS employs 12-bit analog-to-digital converters for the digitization process which causes a noise floor to appear in the frequency domain at -74dB. As the converters used have an analog input voltage range of 2V then a least significant bit (LSB) corresponds to an analog voltage of

$$LSB = \frac{2}{2^{12}} \approx 0.5\text{mV} \tag{4}$$

It is difficult to try and keep noise levels below this value especially in a high speed mixed signal system. At present noise on the analog inputs along with the fact that the converters accept a bipolar analog input degrades the effective number of bits of the digitization process to 9 which raises the noise floor to -54dB.

Once the high frequency components of the signals being digitized fall below the noise floor then the transadmittance function can no longer be determined. The lower of the two frequencies at which the voltage and current magnitude spectra fall below the noise floor determines the bandwidth over which the transadmittance function magnitude can be determined. To ensure that this bandwidth is large enough the following approaches can be used to increase the frequency at which the voltage and current magnitude spectra drop below the noise floor.

1. Increase the vertical resolution used during the digitization process
2. Increase the magnitude of the high frequency components relative to the lower frequency ones for the signal being digitized

Increasing the vertical resolution lowers the quantization noise floor but is not an option as high resolution analog-to-digital converters don't have a high enough sampling rate to avoid aliasing during the digitization process.

The second option can be realized by reducing the rise time and/or fall time of the voltage impulse which reduces the rate of decay of the magnitude spectrum as shown in Fig. 2. The TICMS uses a 1/10μs waveshape impulse as opposed to the

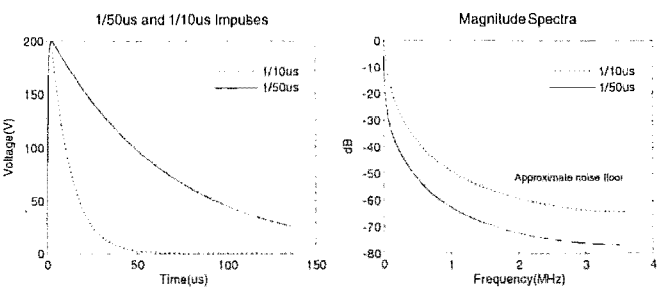

Fig. 2. Impulses in the time and frequency domains

standard 1.2/50μs waveshape that is often used for transformer impulse testing. Further increases in the transadmittance function bandwidth can be achieved by high pass filtering the analog transients prior to digitization and adjusting the attenuation so that the filtered signals take up the full-scale input voltage range of the converters. This technique is implemented in the TICMS as shown in Fig. 3 where an RC high pass filter and an RL shunt are used to attenuate the large magnitude low frequency components which prevents them from taking up much of the dynamic range. As the roll-off of the RC filter is only 20dB/decade, attenuated components (other than DC) of the magnitude spectrum of the filtered impulse are still above the noise floor. This makes it possible for the TMS320C31 DSP used in the TICMS [1] to undo the effects of the filter by digitally dividing the filtered impulse magnitude spectrum by the RC filter transfer function as discussed later. This ensures that the transadmittance function can still be determined at the lower frequencies. The result of filtering the 160V 1/10μs impulse used to determine the transadmittance function of a 7.5kVA 11kV/230V distribution transformer is shown in Fig. 4 where V_{in} represents the magnitude spectrum of the filtered impulse and V_{imp} represents magnitude spectrum of the input impulse $v_{imp}(t)$, that is determined digitally as discussed later. If $v_{imp}(t)$ had been digitized directly without the use of high pass filtering then the -54dB noise floor would have limited the bandwidth to 1.4MHz as indicated in Fig. 4. This would limit the bandwidth of the transadmittance function to 1.4MHz. The magnitude spectrum of $v_{imp}(t)$ is offset from that of $v_{in}(t)$ due to the voltage divider made from R1 and R2 in Fig. 3.

On-line testing in the lab is being performed using the test setup illustrated in Fig 3. During these tests the transformer is energised using a mains supply and the impulse is capacitively coupled onto the HV terminal of the primary winding. The high pass filter prevents the large 50Hz component from taking up dynamic range. Because energising the transformer changes the self and mutual inductance values in Fig. 1, the transadmittance function shape differs. On-line results are being presented in a forth coming publication.

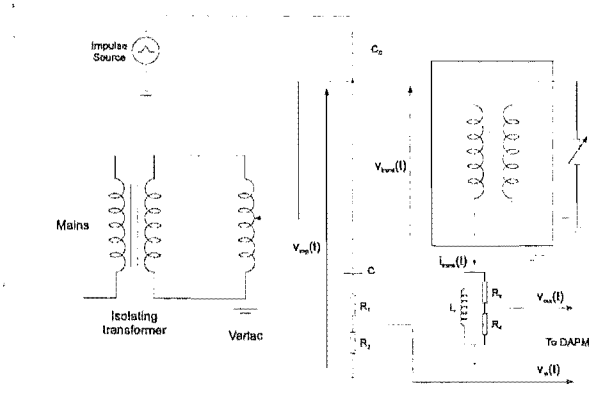

Fig. 3. On-line test configuration

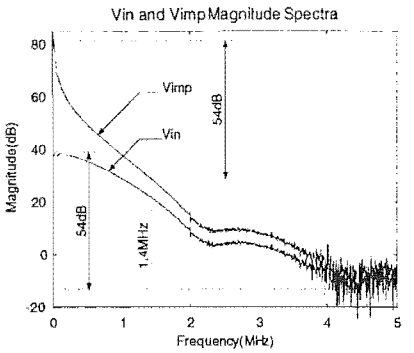

Fig. 4. Increasing the effective dynamic range using analog high pass filtering

IV. DIGITAL SIGNAL PROCESSING

After both analog transients have been digitized the TICMS applies an FFT algorithm to transfer the captured time domain data into the frequency domain so that the transadmittance function can be determined.

A. FFT Implementation

During data acquisition 1024 samples are taken on each channel at a sampling rate of 10MHz. Samples are therefore taken over a time record of 1024 × (1/10MHz) = 102.4μs which is long enough to ensure that both the filtered voltage and current signals have decayed to zero. As no truncation takes place then the time domain signals do not have to be windowed to avoid spectral leakage.

A radix-2 decimation-in-time (DIT) fast Fourier transform (FFT) algorithm is used to determine the discrete Fourier transform (DFT) of $v_{in}(t)$ and $v_{out}(t)$ in Fig. 3. The input data is bit reversed prior to being transformed so that bit reversing doesn't have to be used to determine the twiddle factor powers.

The C code written to implement this algorithm on the DSP assumes a complex input so that the same code can be used to perform an inverse DFT. In transforming a real signal it is therefore necessary to set the imaginary part to zero. However this approach is inefficient as the multiplications involving the imaginary part will still be performed even though it is zero. To avoid this inefficiency the TICMS forms a complex time function by using $v_{in}(t)$ for the real part and $v_{out}(t)$ for the imaginary part. Transforming the complex time function then results in both $v_{in}(t)$ and $v_{out}(t)$ being transformed simultaneously. This leads to a considerable increase in the computational efficiency as the FFT algorithm doesn't have to be used a second time.

The use of the complex time function requires that a sorting algorithm be used to extract the spectra of $v_{in}(t)$ and $v_{out}(t)$ as they are related to the real and imaginary parts of the complex

time function spectrum as follows [6]

$$V_{in}(f) = \frac{R(f)}{2} + \frac{R(N-f)}{2} + j\left[\frac{I(f)}{2} - \frac{I(N-f)}{2}\right] \quad (5)$$

$$V_{out}(f) = \frac{I(f)}{2} + \frac{I(N-f)}{2} - j\left[\frac{R(f)}{2} - \frac{R(N-f)}{2}\right] \quad (6)$$

where N is the number of samples and $V_{in}(f)$ and $V_{out}(f)$ are the spectra of $v_{in}(t)$ and $v_{out}(t)$ respectively. This sorting procedure only requires a total of 2N+4 additions as the real and imaginary parts of $V_{in}(f)$ and $V_{out}(f)$ are symmetrical about N/2. This represents a significant computational saving as the use of the FFT algorithm a second time would require an additional $(N/2)\log_2 N$ complex multiplications and $N\log_2 N$ complex additions. Following the sorting procedure the spectra of $v_{in}(t)$ and $v_{out}(t)$ are converted into polar format.

B. Transadmittance Function Magnitude Determination

To determine the transadmittance function it is necessary to determine $V_{trans}(f)$ and $I_{trans}(f)$ which denote the frequency domain equivalents of the time domain quantities in Fig. 3.

To determine $|V_{trans}(f)|$ the TICMS first determines $|V_{imp}(f)|$ in Fig. 3 by dividing $|V_{in}(f)|$ at each discrete frequency by the magnitude of the transfer function of the RC high pass filter so that

$$\left|V_{imp}(f)\right| = \frac{\left|V_{in}(f)\right|\sqrt{1+\left(f/f_{12}\right)^2}}{f/f_2} \quad (7)$$

where

$$f_2 = \frac{1}{2\pi R_2 C} \quad , \quad f_{12} = \frac{1}{2\pi(R_1+R_2)C} \quad (8)$$

The magnitude spectra of $V_{in}(f)$ and $V_{imp}(f)$ are shown in Fig. 4.

Next $V_{trans}(f)$ is determined at each discrete frequency as follows

$$V_{trans}(f) = V_{imp}(f) - \frac{(R_3+R_4)V_{out}(f)}{R_4} \quad (9)$$

By converting (9) to rectangular form and then taking the magnitude of the result it can be shown that

$$\left|V_{trans}(f)\right| = \left[\left|V_{imp}(f)\right|^2 + \left(\frac{(R_3+R_4)\left|V_{out}(f)\right|}{R_4}\right)^2 - \frac{2\left|V_{imp}(f)\right|(R_3+R_4)\left|V_{out}(f)\right|\cos\left[\psi(f)\right]}{R_4}\right]^{1/2} \quad (10)$$

where

$$\psi(f) = \alpha - \beta \quad (11)$$

and α and β are the phase of $V_{imp}(f)$ and $V_{out}(f)$ respectively and are both a function of frequency.

The magnitude of the RL shunt is then used to determine $|I_{trans}(f)|$ as follows

$$\left|I_{trans}(f)\right| = \frac{\left|V_{out}(f)\right|}{R_4}\frac{\sqrt{1+\left(f/f_c\right)^2}}{f/f_c} \quad (12)$$

where

$$f_c = \frac{R_3+R_4}{2\pi L} \quad (13)$$

Therefore in summary the TICMS determines the transadmittance function magnitude by dividing $|I_{trans}(f)|$ by $|V_{trans}(f)|$ at each discrete frequency where $|I_{trans}(f)|$ and $|V_{trans}(f)|$ are given by (12) and (10) respectively.

C. Transadmittance Function Phase Determination

To determine the transadmittance function phase the TICMS subtracts the phase of $|V_{trans}(f)|$ from that of $|I_{trans}(f)|$ where the phase of $|V_{trans}(f)|$ is determined from (9) as follows

$$\arg\left[V_{trans}(f)\right] = \tan^{-1}\left[\frac{\left|V_{imp}(f)\right|\sin\alpha - \left(\frac{R_3+R_4}{R_4}\right)\left|V_{out}(f)\right|\sin\beta}{\left|V_{imp}(f)\right|\cos\alpha - \left(\frac{R_3+R_4}{R_4}\right)\left|V_{out}(f)\right|\cos\beta}\right] \quad (14)$$

From impedance of the RL shunt it is also easily shown that

$$\arg\left[I_{trans}(f)\right] = \beta - \frac{\pi}{2} + \tan^{-1}\left(\frac{f}{f_c}\right) \quad (15)$$

so that the phase of the transadmittance function is determined by subtracting (14) from (15) at each discrete frequency.

V. RESULTS

Off-line testing has been performed (mains supply in Fig. 3 disconnected) on a 7.5kVA 11kV/230V distribution

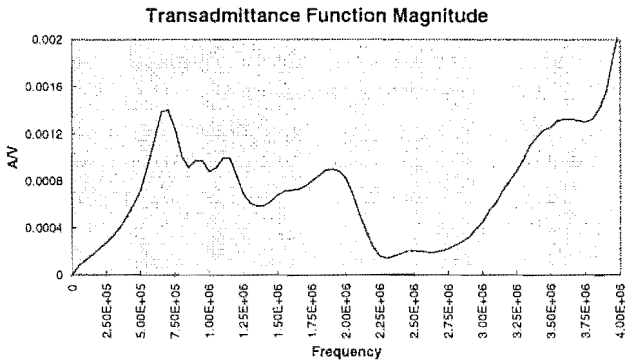

Fig. 5. Transadmittance function magnitude determined by sweep frequency testing

transformer with a layered winding. The primary winding consists of two coils in series wound on opposite legs of a square core. Each coil consists of 34 layers at 205 turns per layer giving a total of about 14000 turns. For this winding type the transadmittance function consists of a series of poles at 700kHz, 950kHz, 1.15MHz and 1.9MHz as shown in Fig. 6.

A sweep frequency test has also been performed on the same transformer by applying sinusoids at 50kHz increments from DC to 3MHz. A 10Ω resistor was used between the neutral terminal of the transformer and ground for measuring the current response. The amplitude of the input and output sinusoids along with their phase difference was recorded at each frequency and the results were used to determine the transadmittance function magnitude by employing a relation similar to (10). Fig. 5 shows the transadmittance function magnitude determined using sweep frequency testing where it can be seen that it is in good agreement with that determined by the TICMS in Fig. 6. This gives confidence in the results produced by the TICMS.

The noise floor in the frequency domain limits the bandwidth of the transadmittance function. The TICMS uses transadmittance function averaging over a user selectable number of acquisitions to reduce the noise over the 2-3MHz range. Averaging has been applied in Fig. 6, resulting in excellent agreement with Fig. 5.

VI. CONCLUSIONS

The signal processing principles used to determine the winding transadmittance function from the analog transients that result from an insulation test have been presented. The

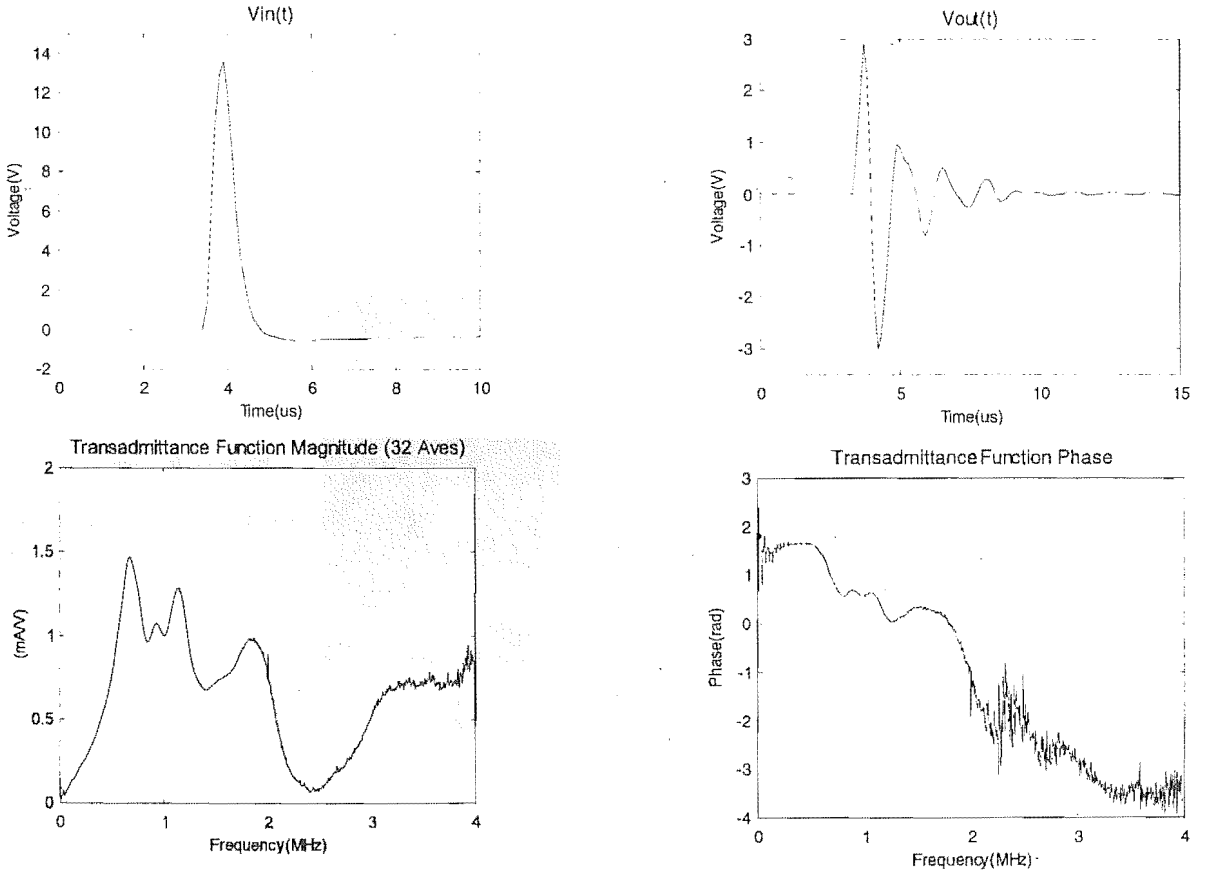

Fig. 6. Results for 7.5kVA 11kV/230V transformer determined by the TICMS

use of high speed data acquisition and a powerful 32-bit floating point DSP has enabled these techniques to be implemented in real-time.

A low voltage 1/10μs impulse has been used to determine the transadmittance function of a 7.5kVA 11kV/230V distribution transformer to 3MHz by using an analog high pass filtering scheme that extends the effective dynamic range of the analog-to-digital converters. A transadmittance function bandwidth of 3MHz should be sufficient detect breakdown between adjacent turns in an EHV transformer [2].

The TICMS has been designed to determine the transadmittance function in real-time as the system is aimed at determining the transadmittance function of a transformer while it is in service. This is being implemented in the TICMS by capacitively coupling the low voltage excitation onto the transformers sinusoidal input. The RL shunt can be used to determine the current response in an on-line situation as its reactance is designed to be negligible at 50Hz. The RC filter and RL shunt attenuate the large 50Hz components, preventing them from taking up any dynamic range when testing an energised transformer.

At present low voltage impulse testing is being used to determine the transadmittance function both off-line and on-line. Field trials which involve testing a fully energised transformer in service are currently being planned. The system is also being extended to allow natural disturbances and power system transients to be used as an excitation source. This will allow the initiation of a test upon the arrival of a transient.

Artificial faults have been placed in the winding of the 7.5kVA transformer to establish relationships between the location and size of the fault and the corresponding changes in the transadmittance function [2]. The key issue in using this technique for identifying insulation condition changes is to be able to identify both gradual and/or sudden changes in the frequency signature. Consequently the exact or absolute value of the transadmittance function is not as important as being able to identify differential changes in the transadmittance function both in the long and short term. It is however important to have a high degree of confidence that the signatures obtained are a reasonable representation of the transadmittance function.

VII. ACKNOWLEDGMENTS

The financial assistance of the University of Canterbury Doctoral scholarship for G.J.Lavery is gratefully acknowledged. The authors would also like to thank Southpower for donating transformers for testing.

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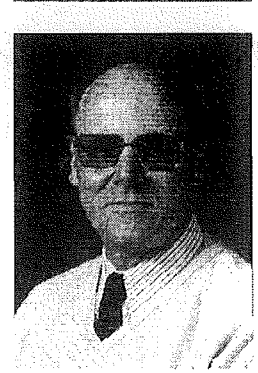
[7] H.Baher, *Analog and Digital Signal Processing*, John Wiley and Sons, 1990

IX. BIOGRAPHIES

Grant J. Lavery received a BE degree with first class honors in electrical engineering from the University of Canterbury New Zealand in 1993. He is currently pursuing postgraduate research leading to a Ph.D. degree at the University of Canterbury N.Z.



Michael B. Dewe received the B.Sc. degree from the University of Capetown South Africa in 1964, and an ME degree from the University of Canterbury New Zealand in 1966. He worked for the Space Division of Hawken Siddeley Dynamics Ltd (now British Aerospace Ltd), U.K., until 1972 where he was Group Leader of Electronic Systems Design. He was a Senior Lecturer at the University of Witwatersand S.A. until taking up a similar post with the University of Canterbury in 1978. In 1981 he joined Wormald Vigilant Ltd. N.Z., where he was Engineering Manager and Associate Director until rejoining the University of Canterbury in 1985. His prime research interests are in the field of applying state-of-the-art techniques to power system instrumentation.

Appendix J

TICMS SCHEMATICS

Included are the hardware schematics for the DAPM, IGM, sampling clock generator modification, and the FPGA internal architecture.

J.1 DAPM

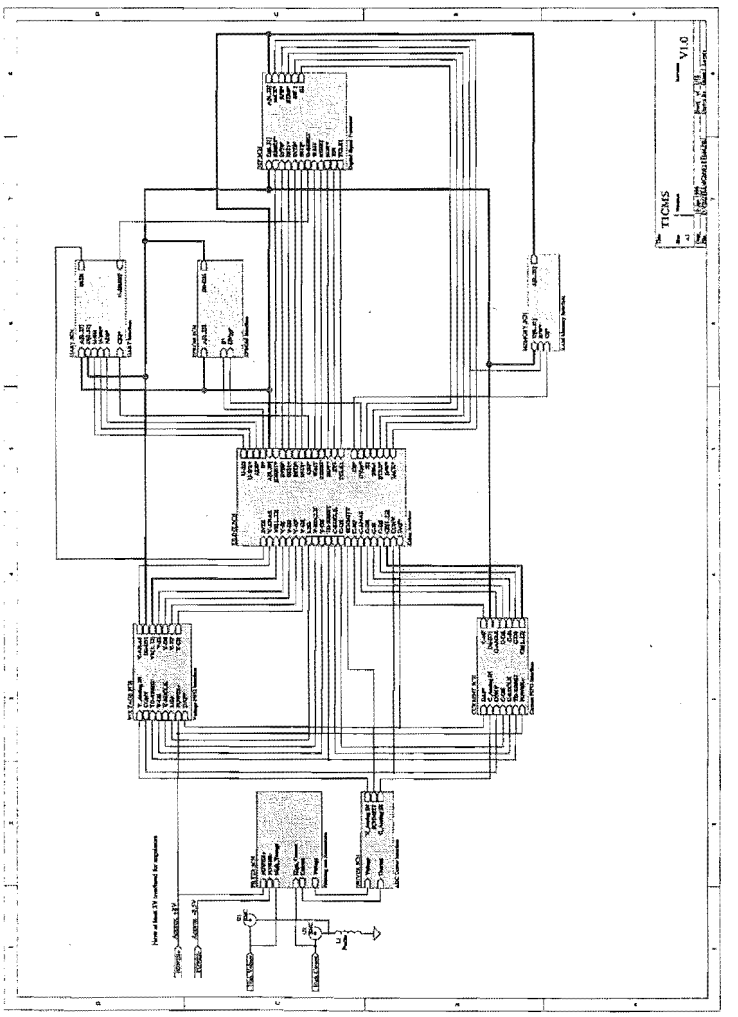


Figure J-1 DAPM top level schematic

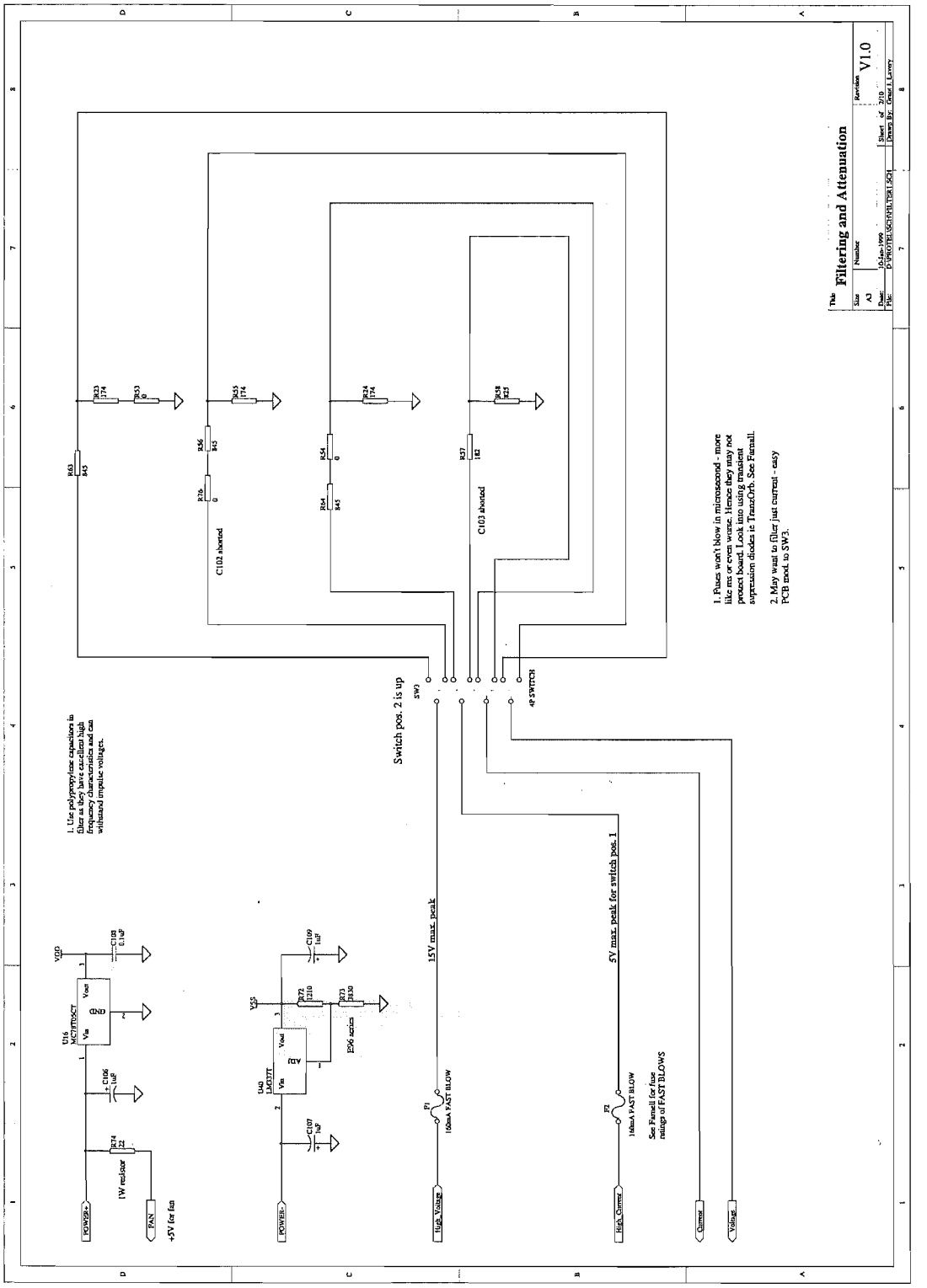


Figure J-2 High pass filtering

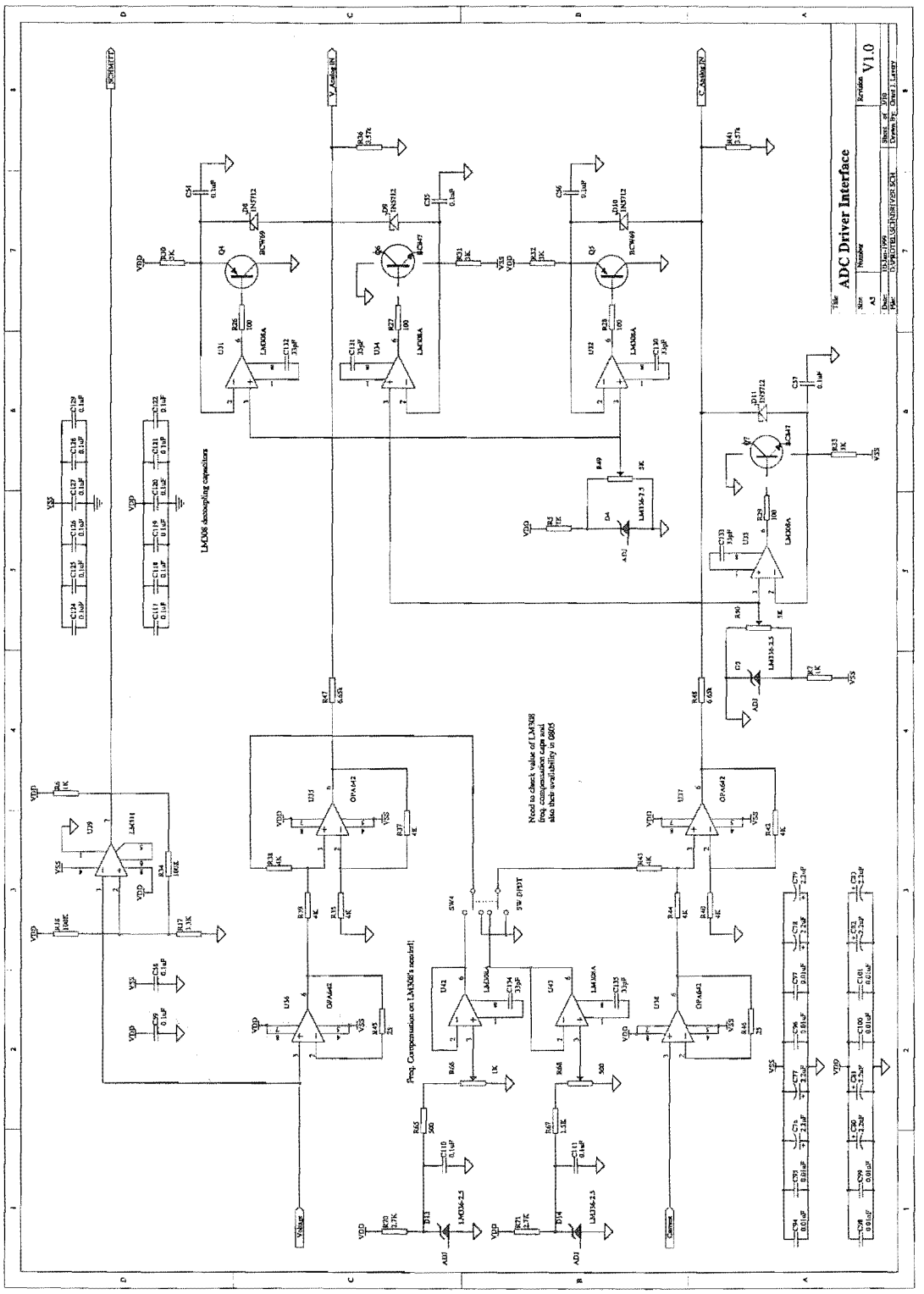


Figure J-3 A/D converter driving electronics

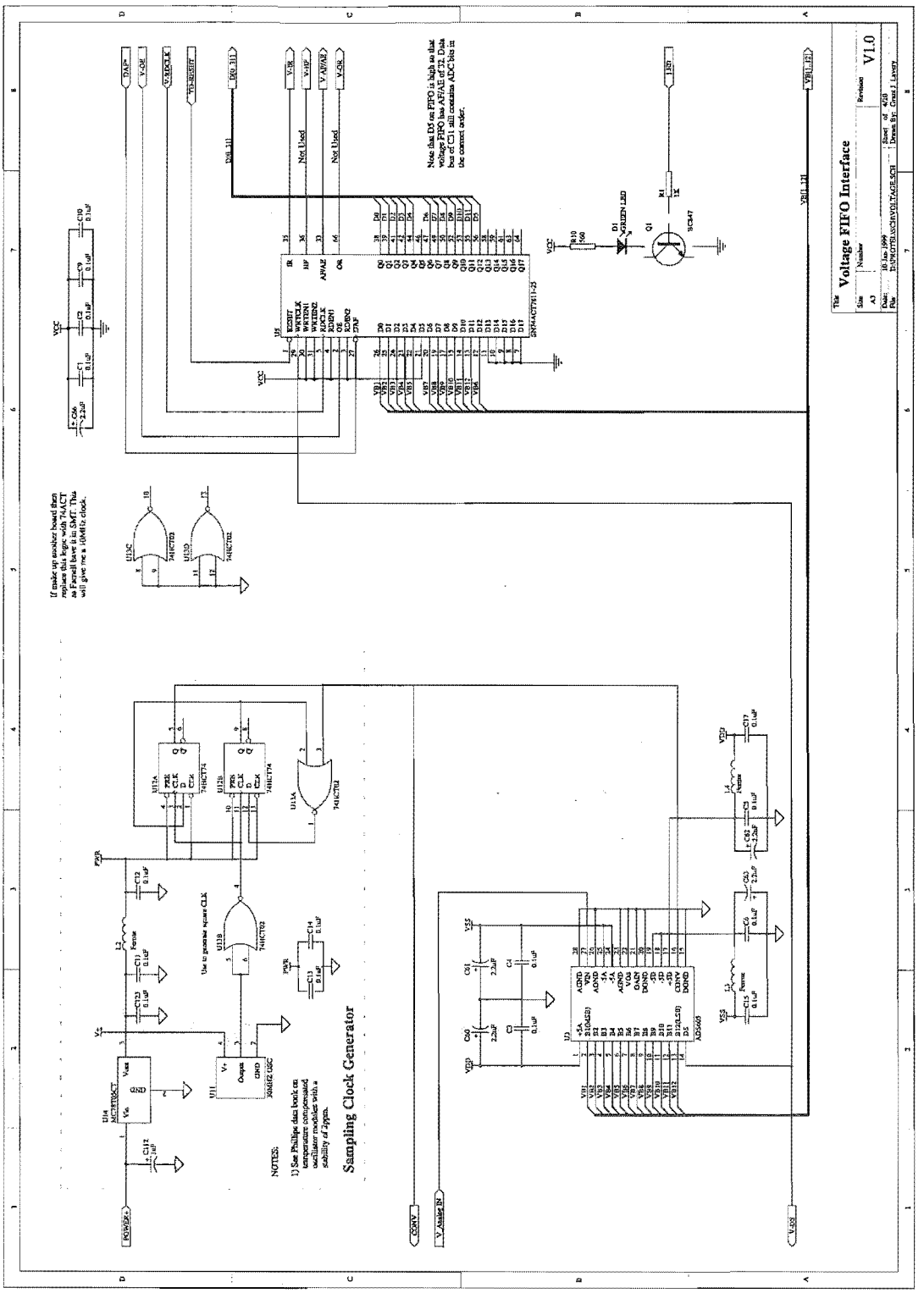


Figure J-4 Voltage channel FIFO interface

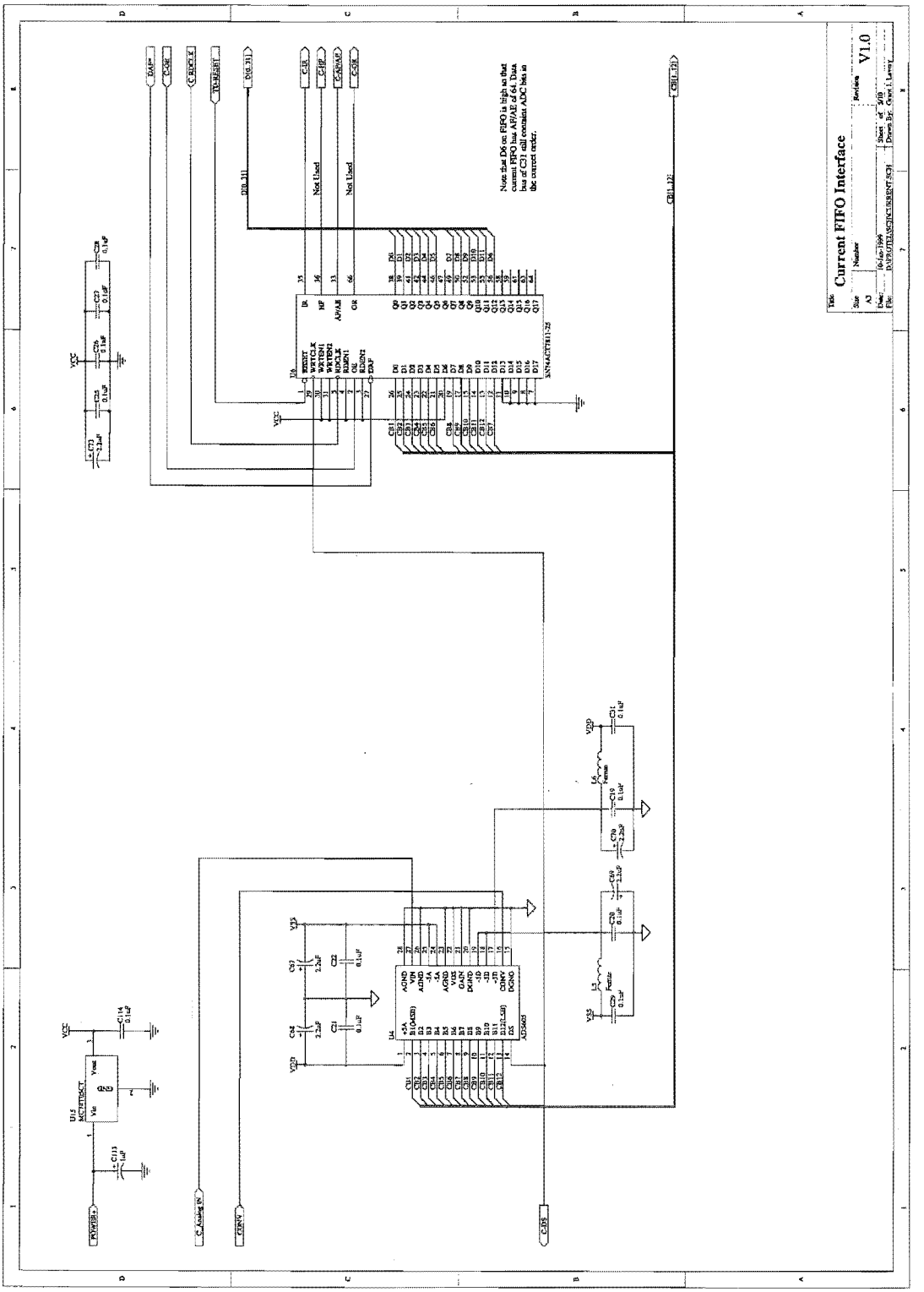


Figure J-5 Current channel FIFO interface

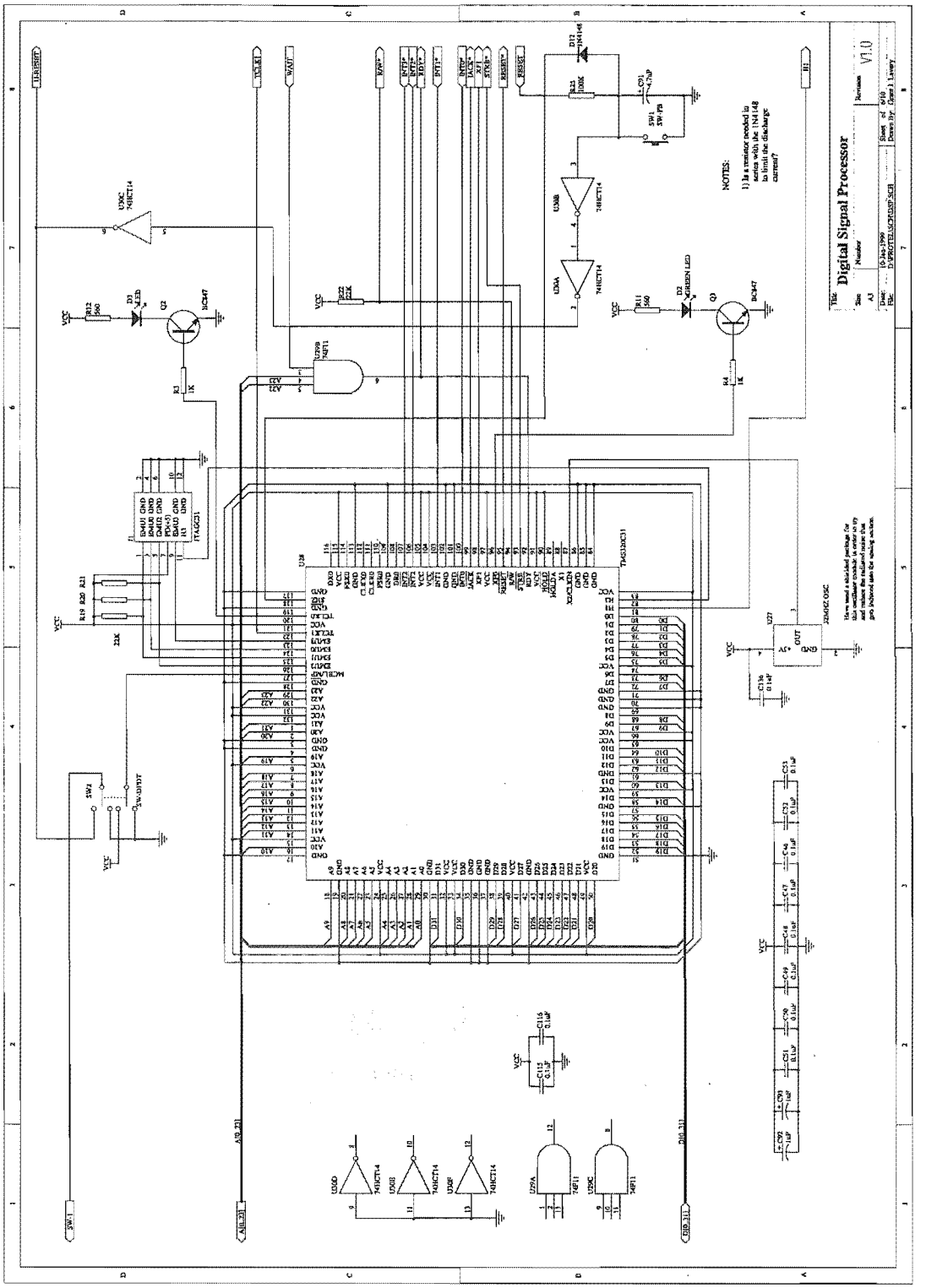


Figure J-6 TMS320C31 DSP interface

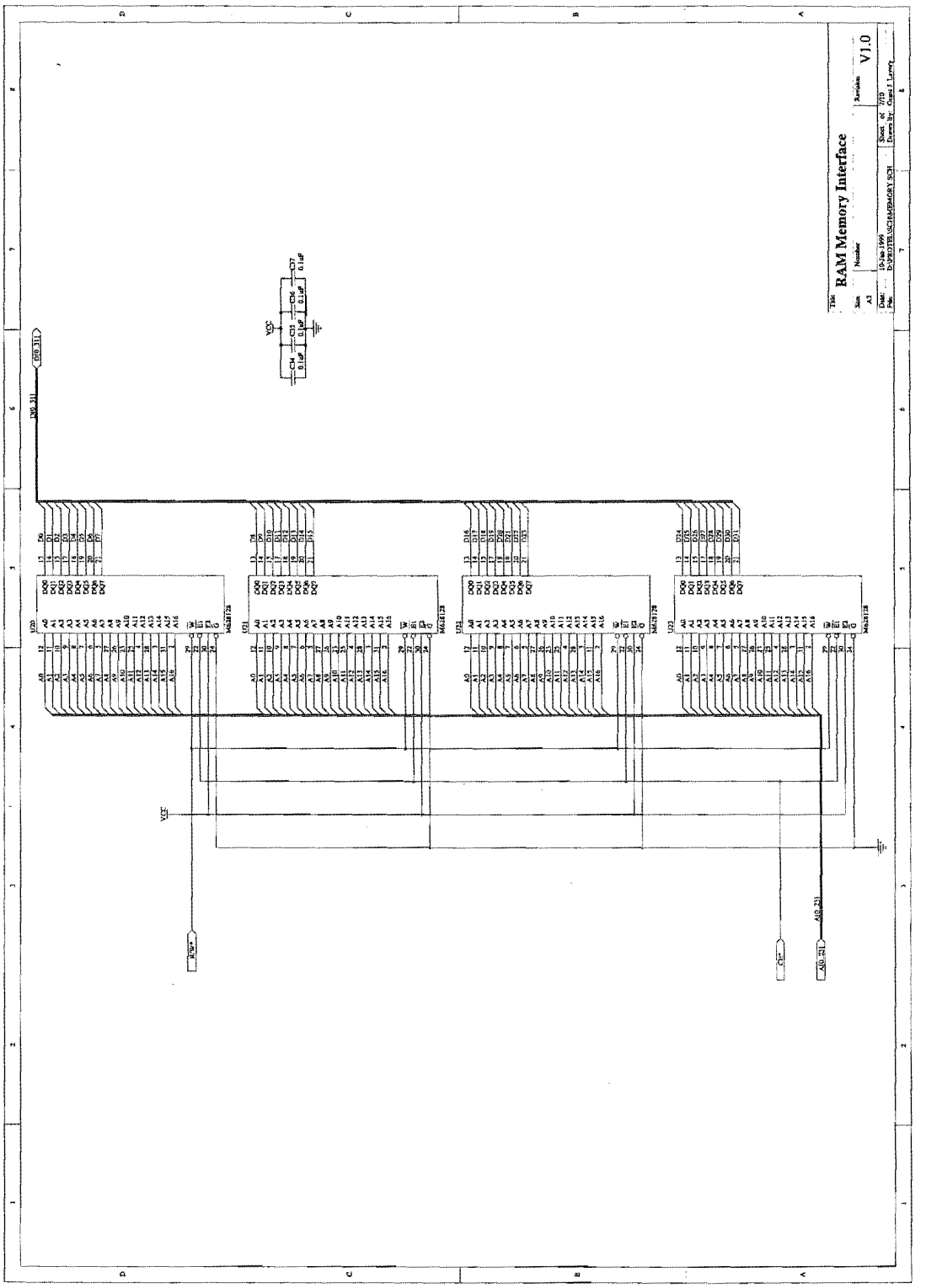


Figure J-7 DAPM static RAM interface

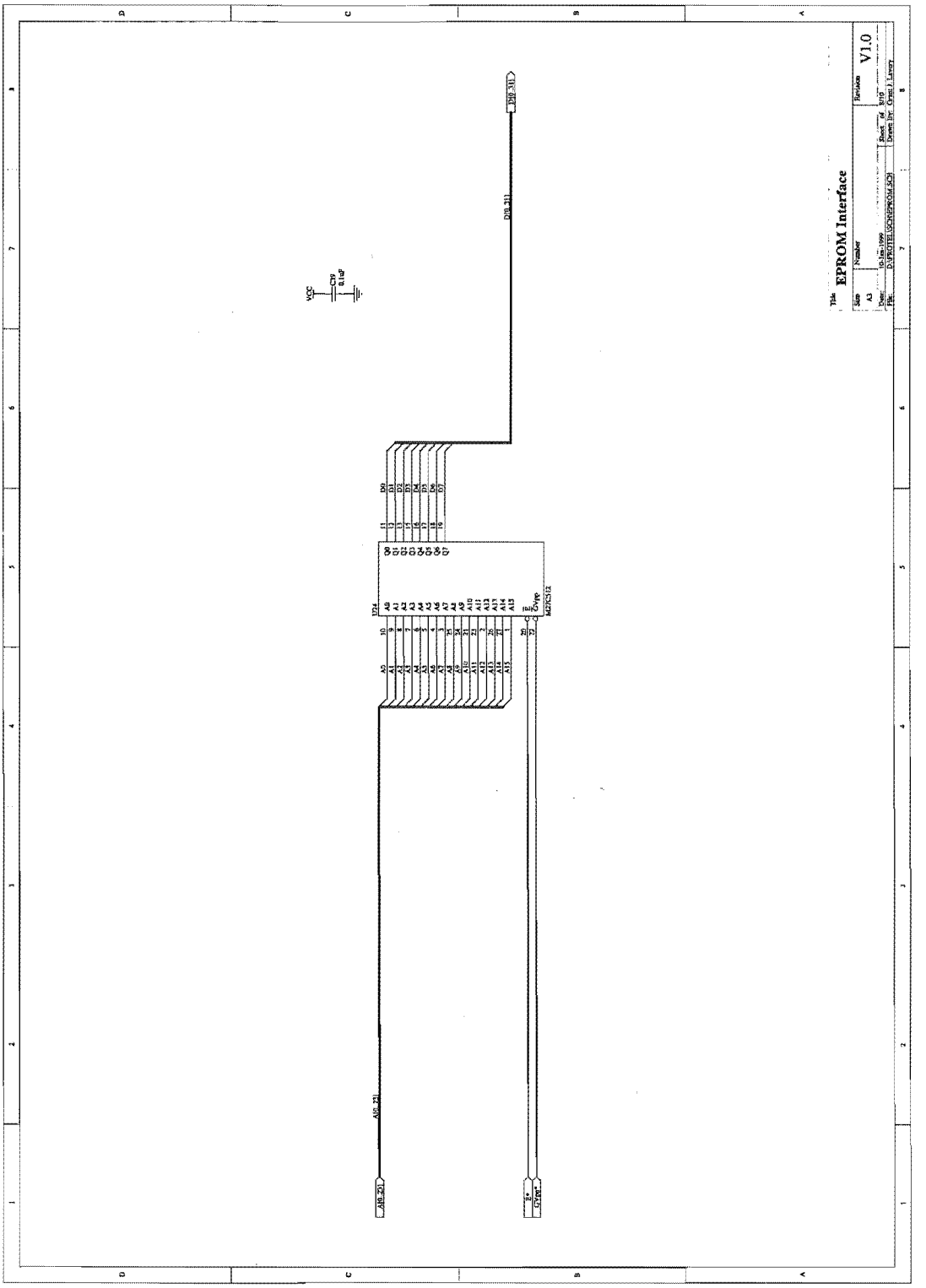


Figure J-8 EPROM interface

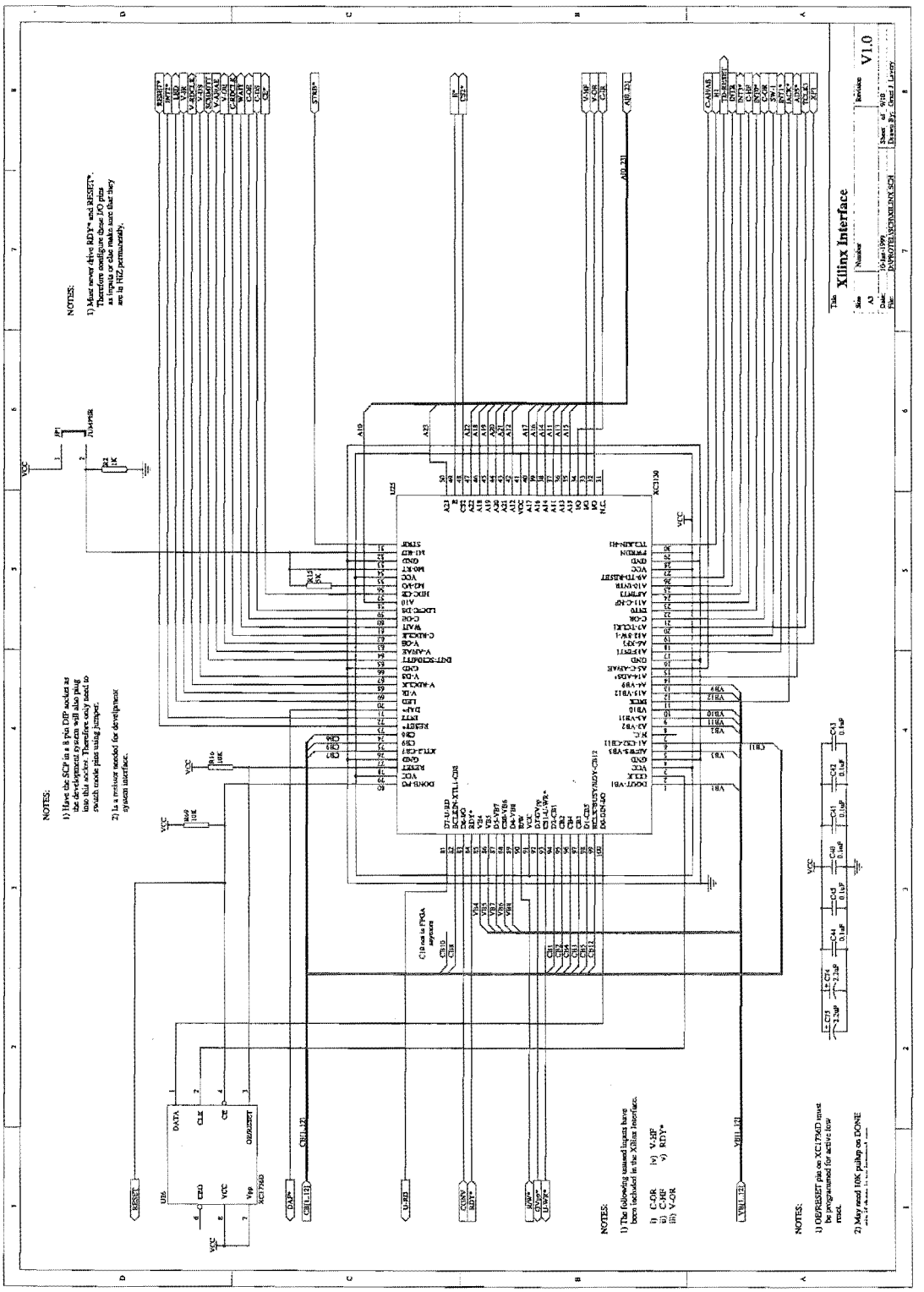


Figure J-9 FPGA interface

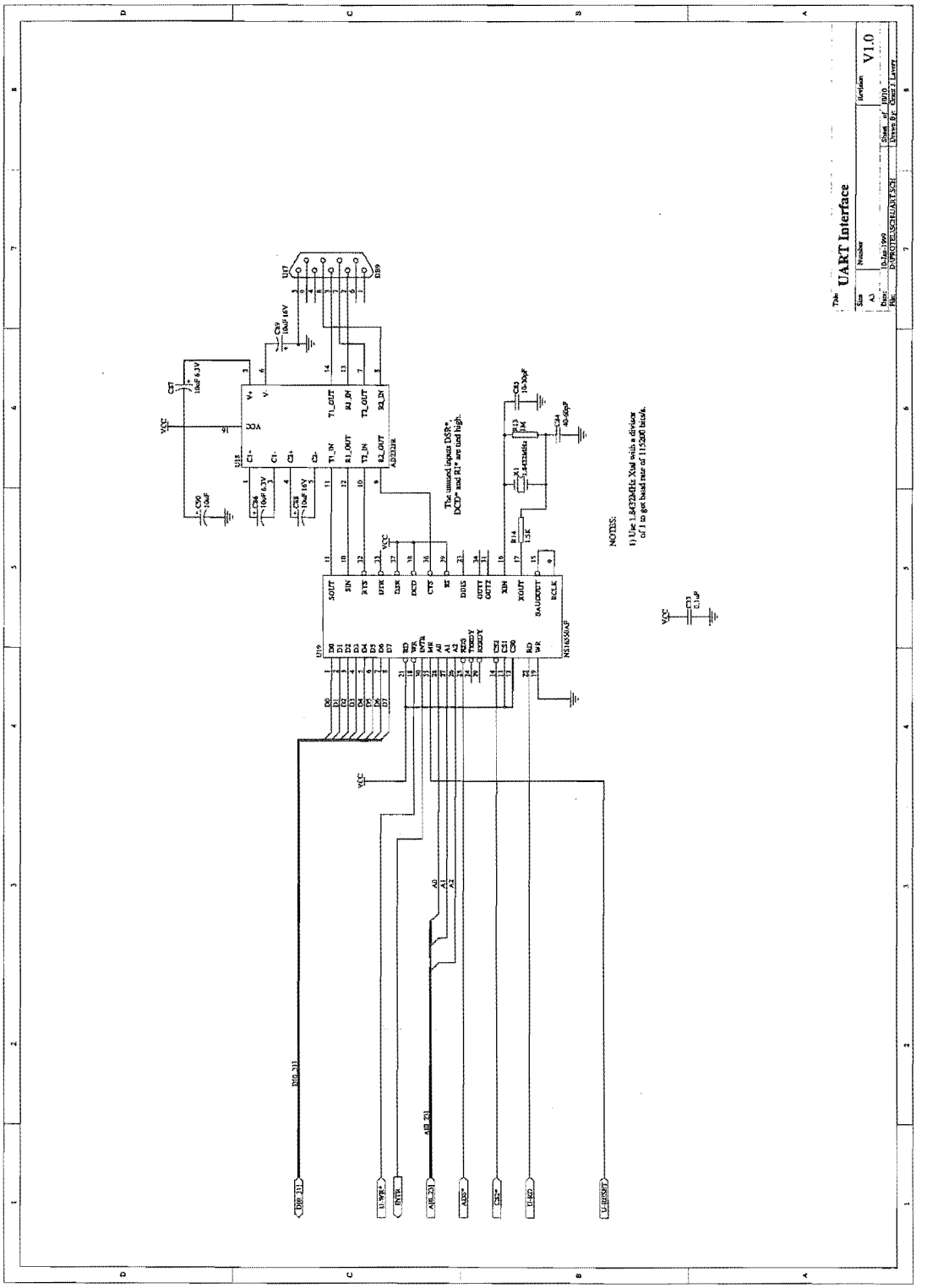


Figure J-10 UART serial interface

J.2 IGM

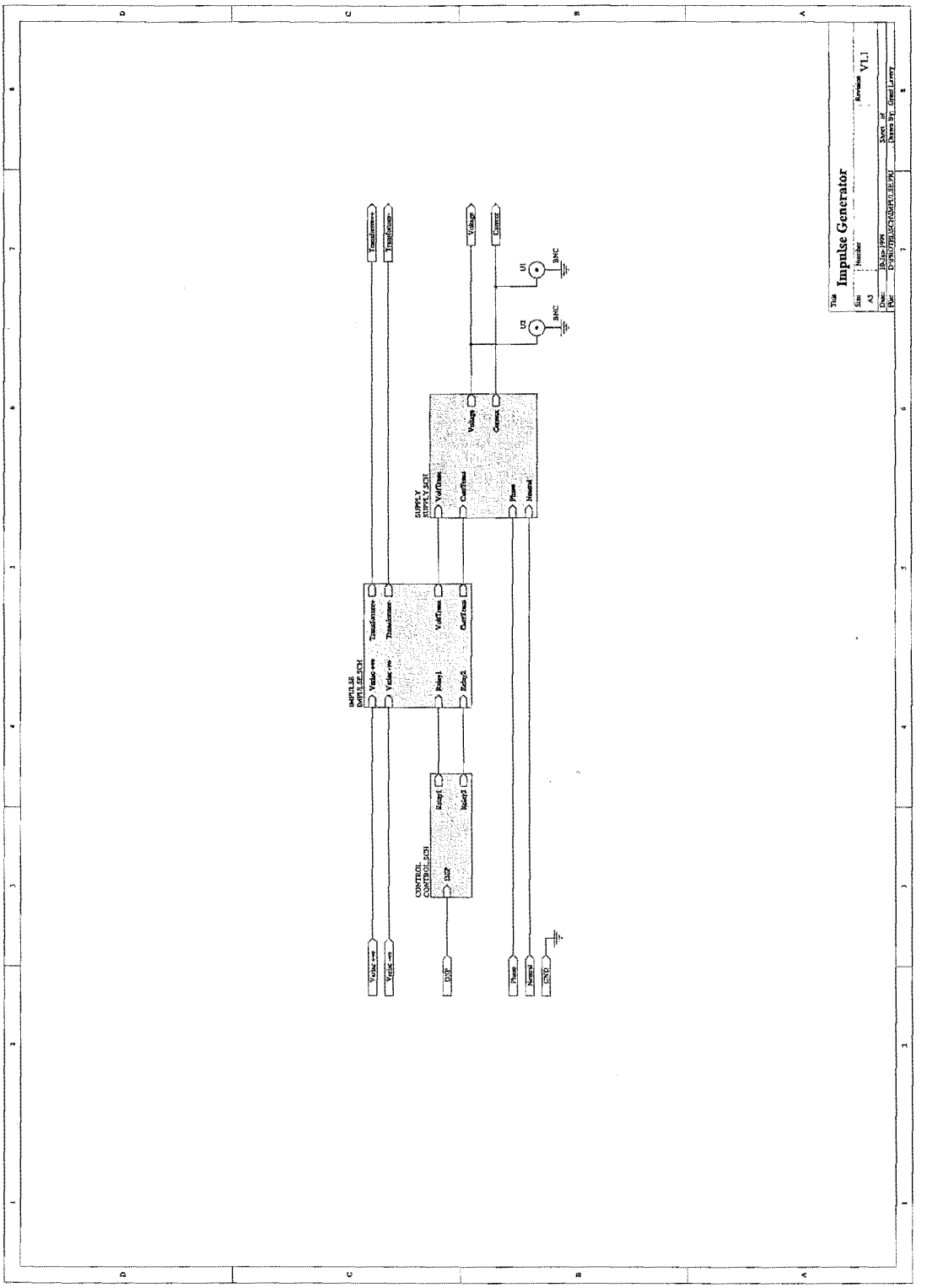


Figure J-11 IGM top level schematic

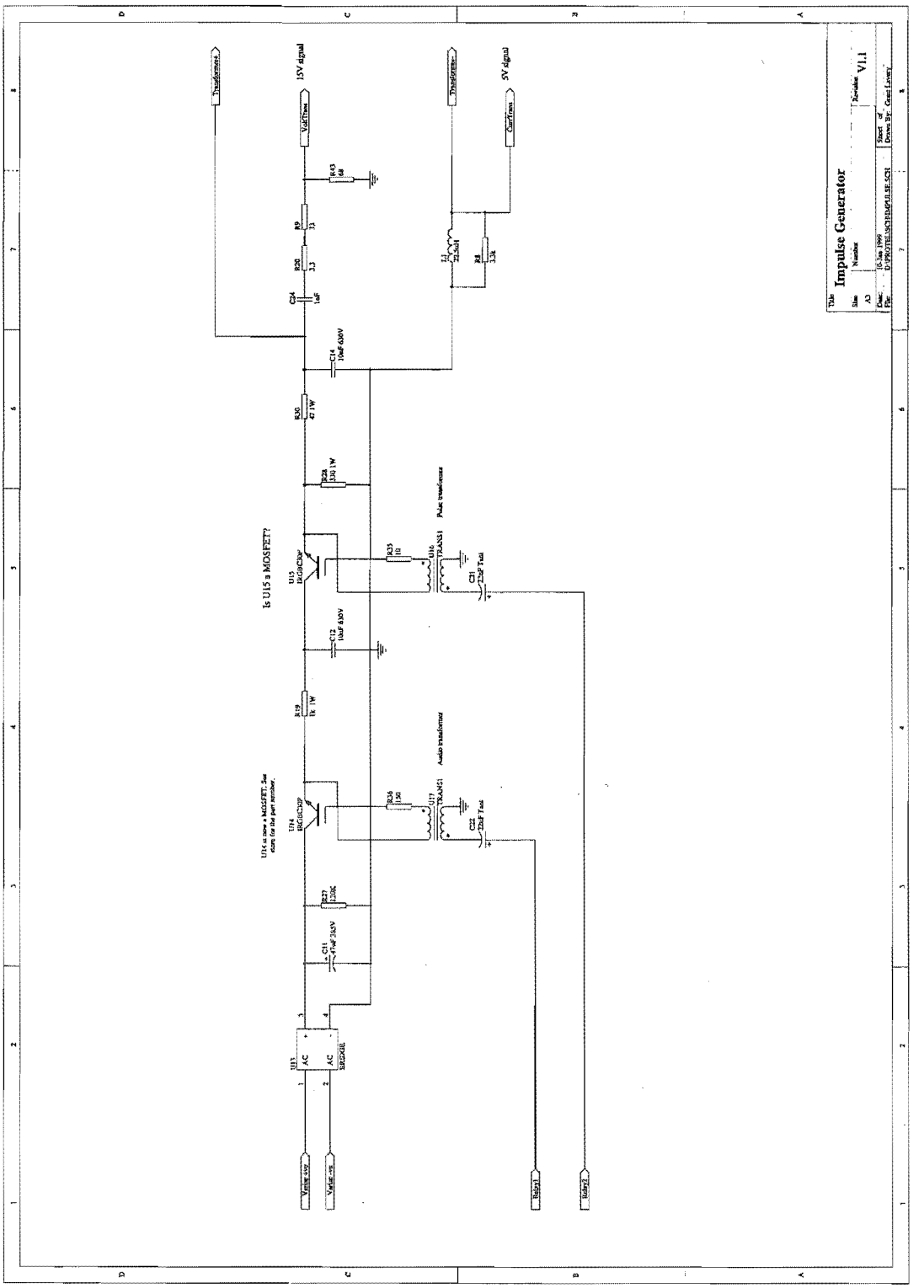


Figure J-12 Impulse generation circuitry

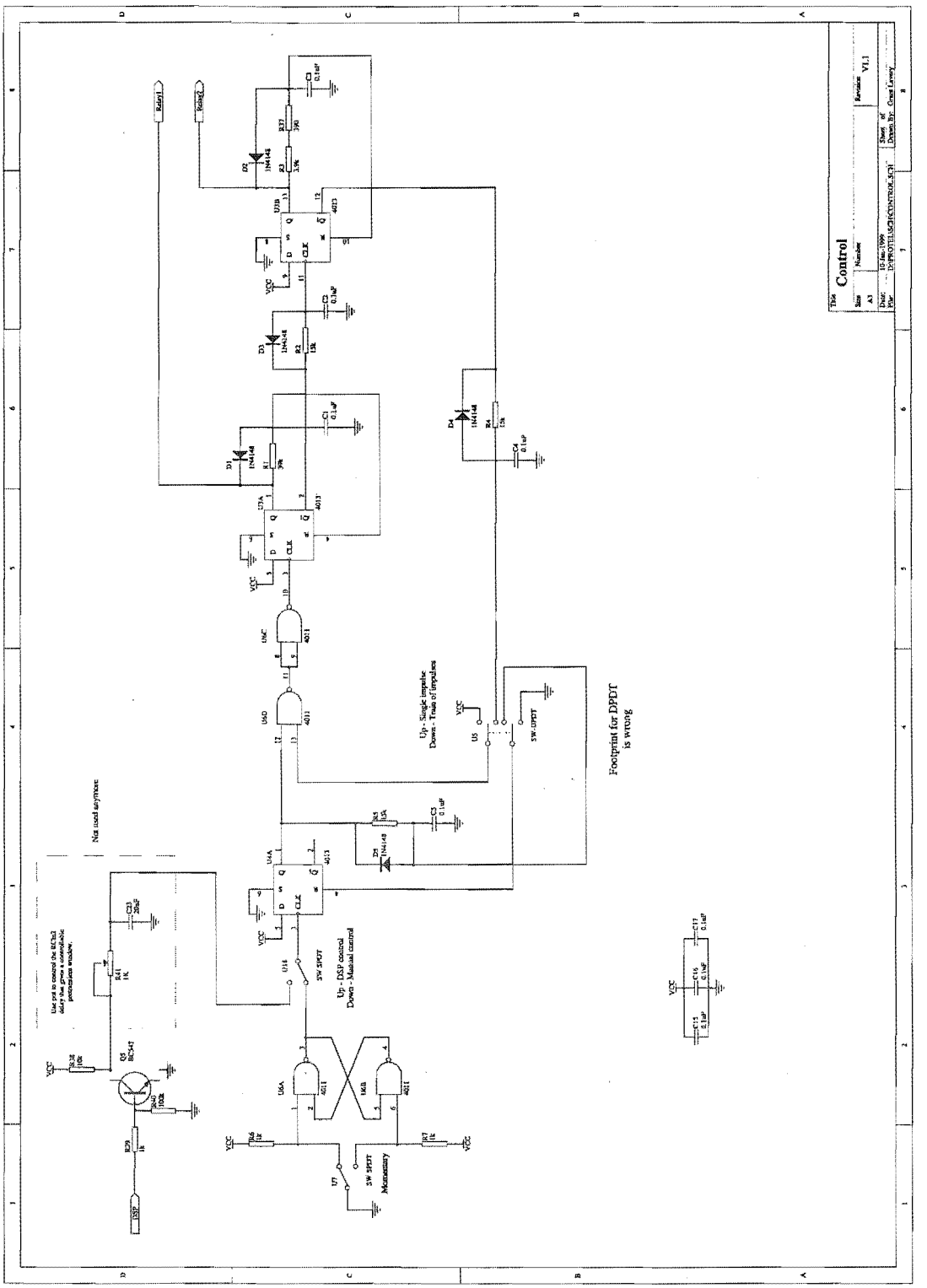


Figure J-13 Control electronics

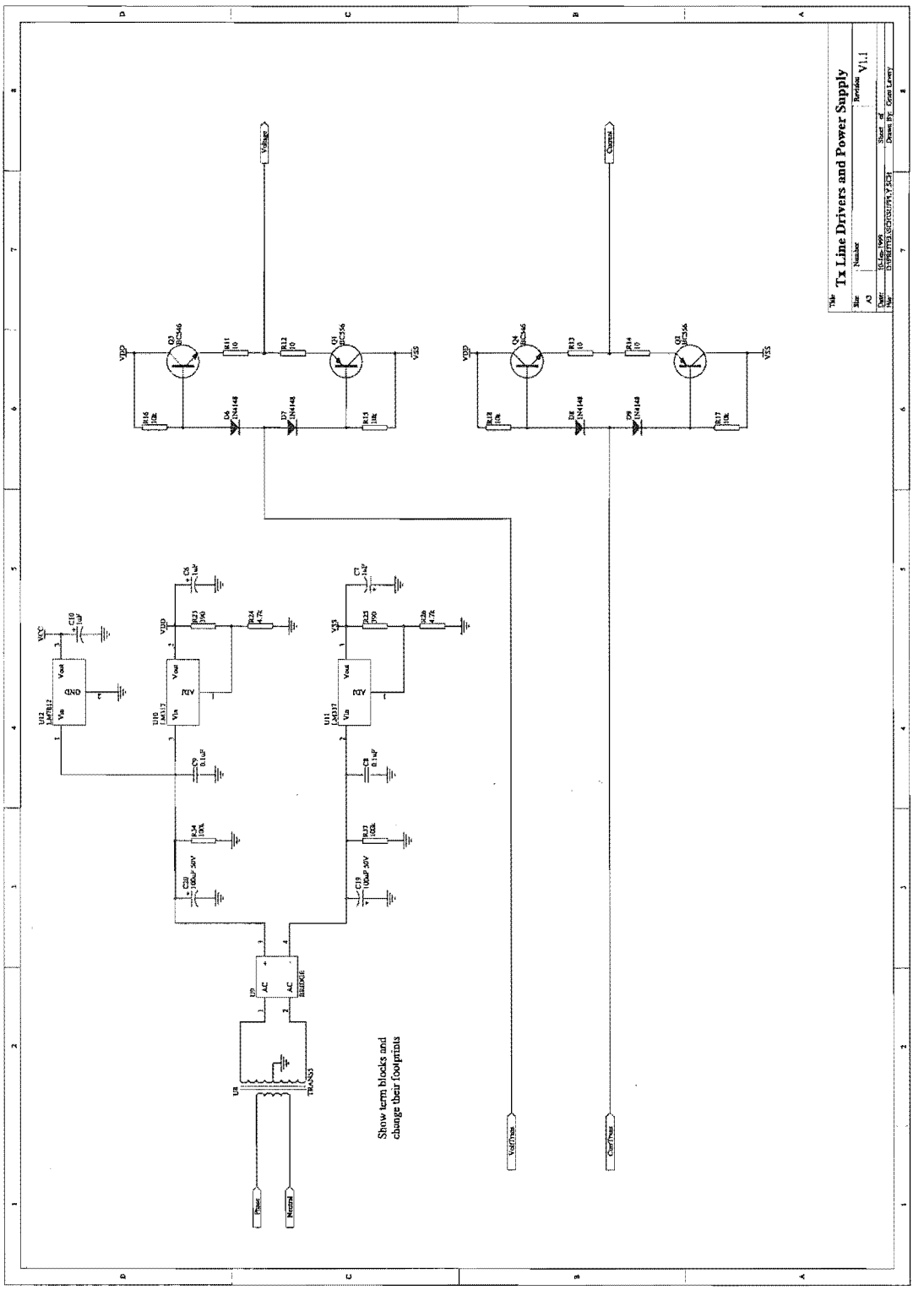


Figure J-14 Power supply

J.3 Sampling Clock Generator

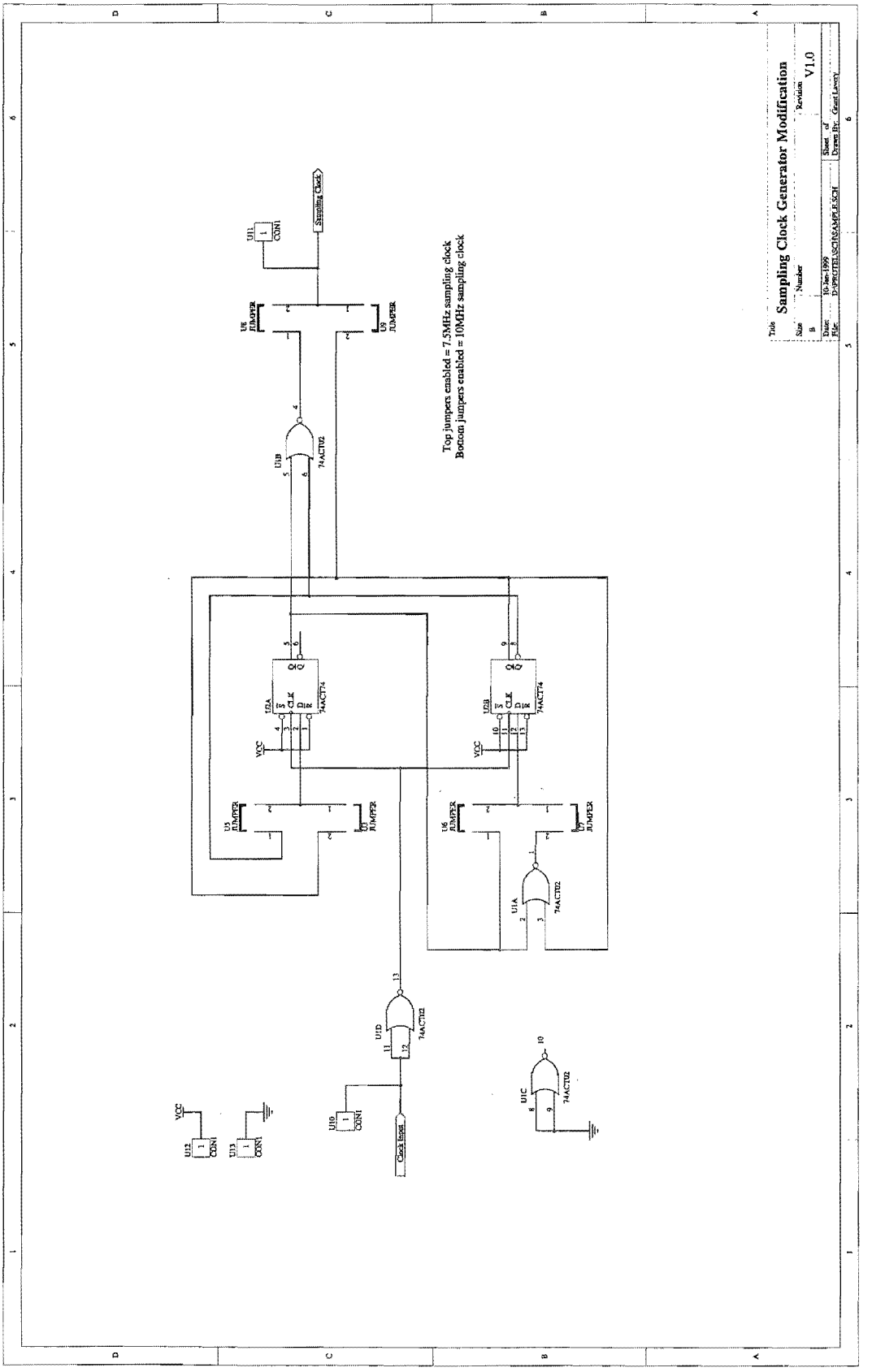


Figure J-15 DAPM sampling clock generator modification

J.4 FPGA

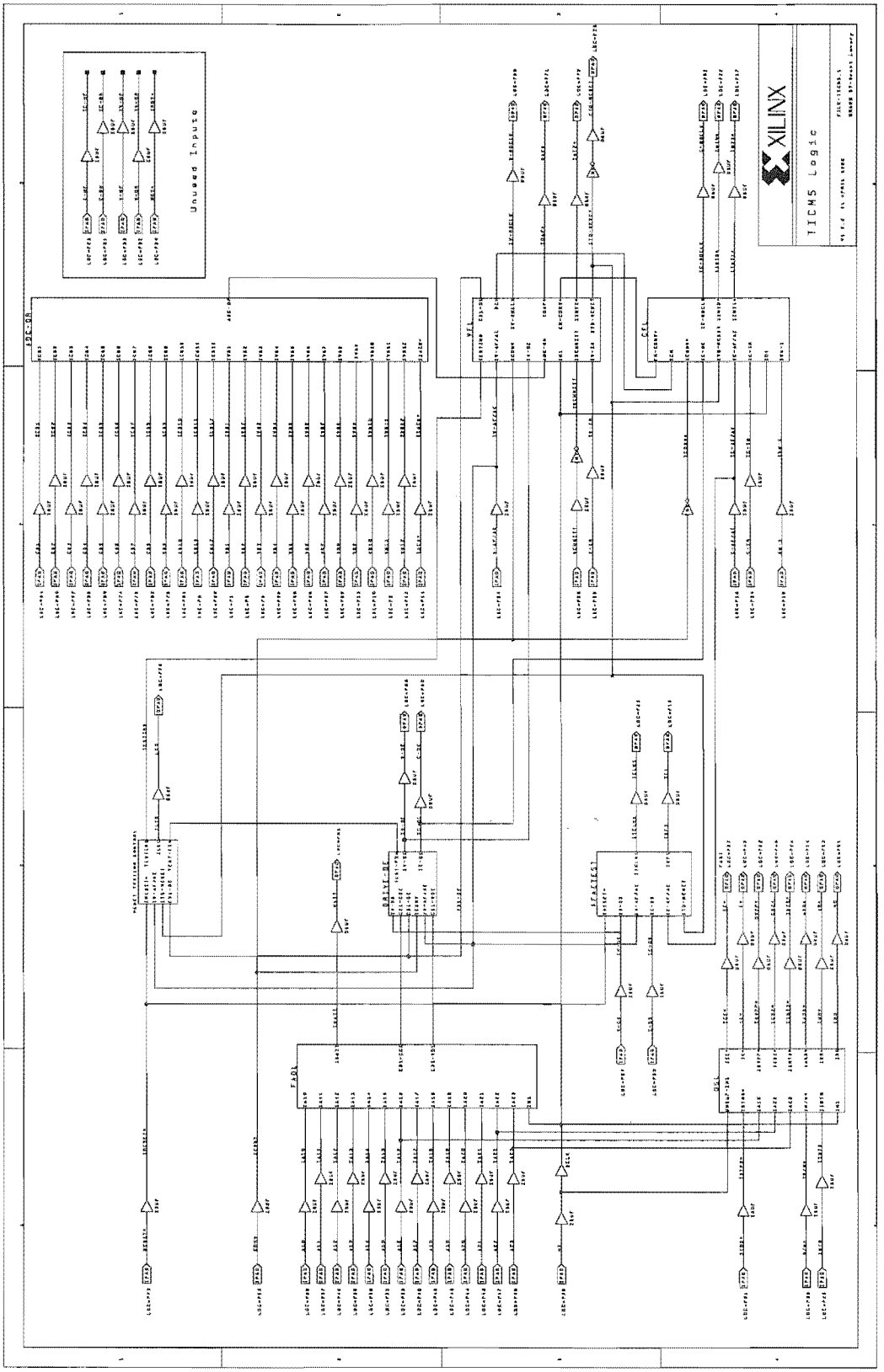


Figure J-16 FPGA top level schematic

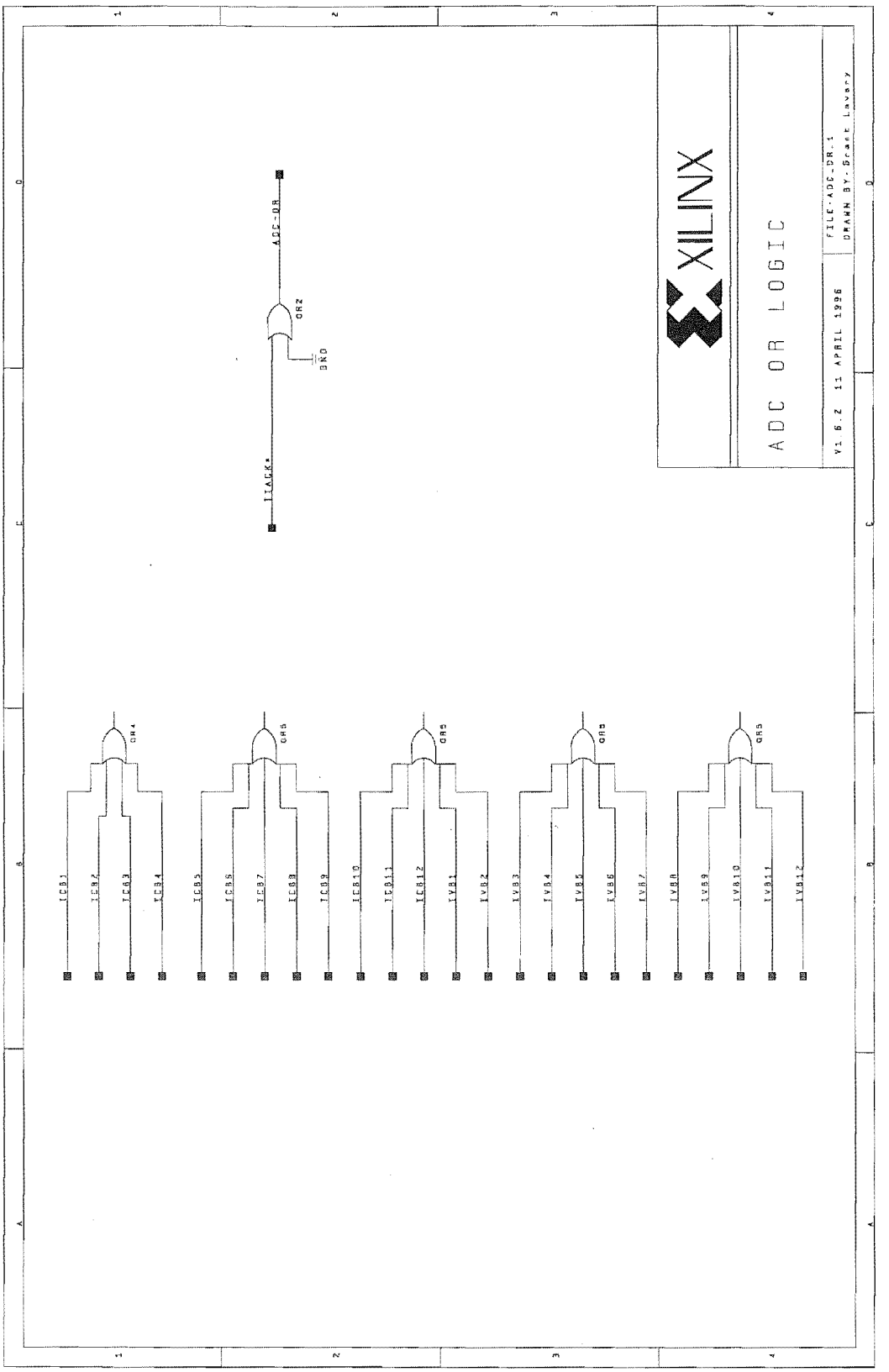


Figure J-17 ADC OR logic

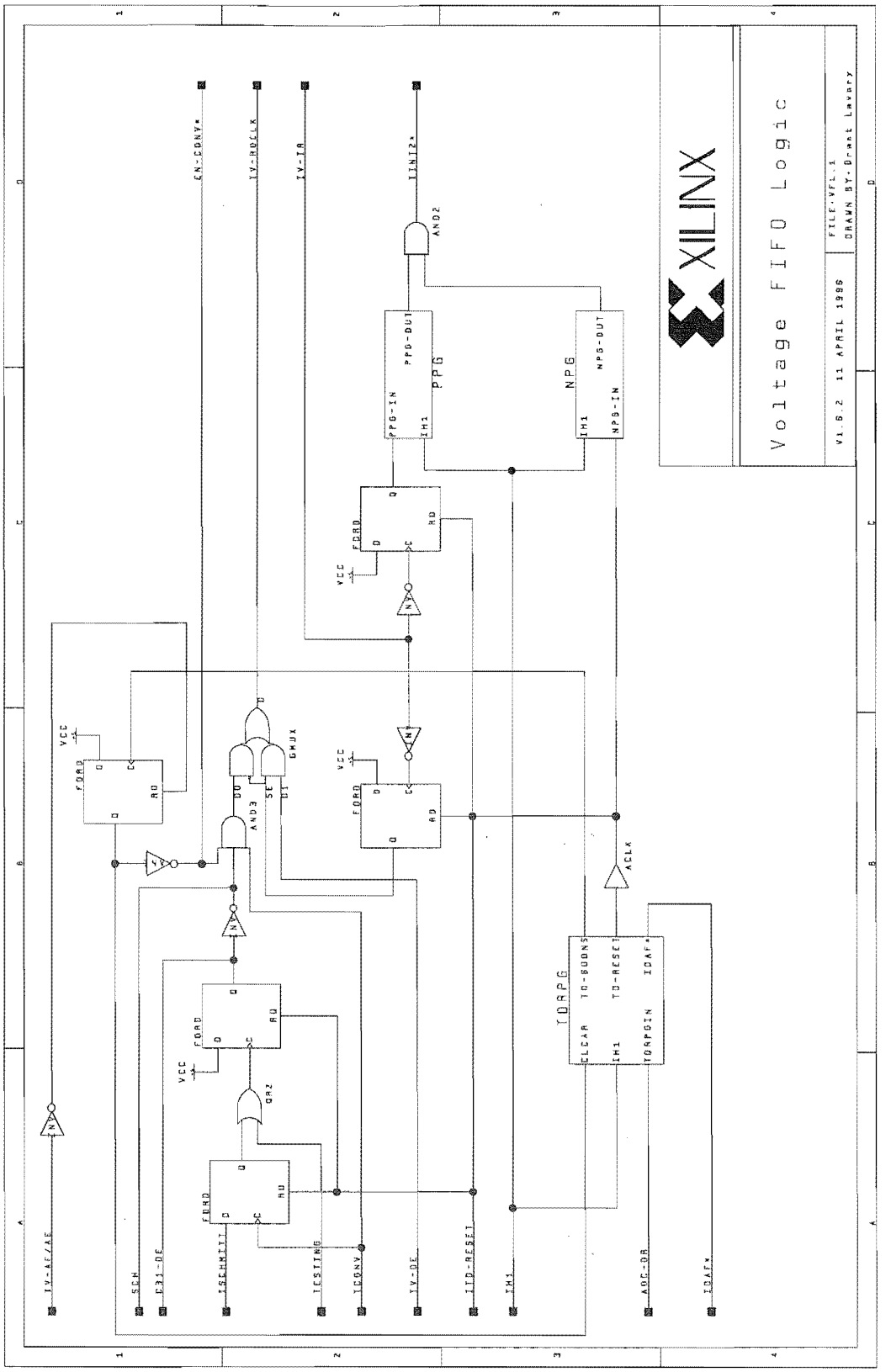


Figure J-18 Voltage channel FIFO logic

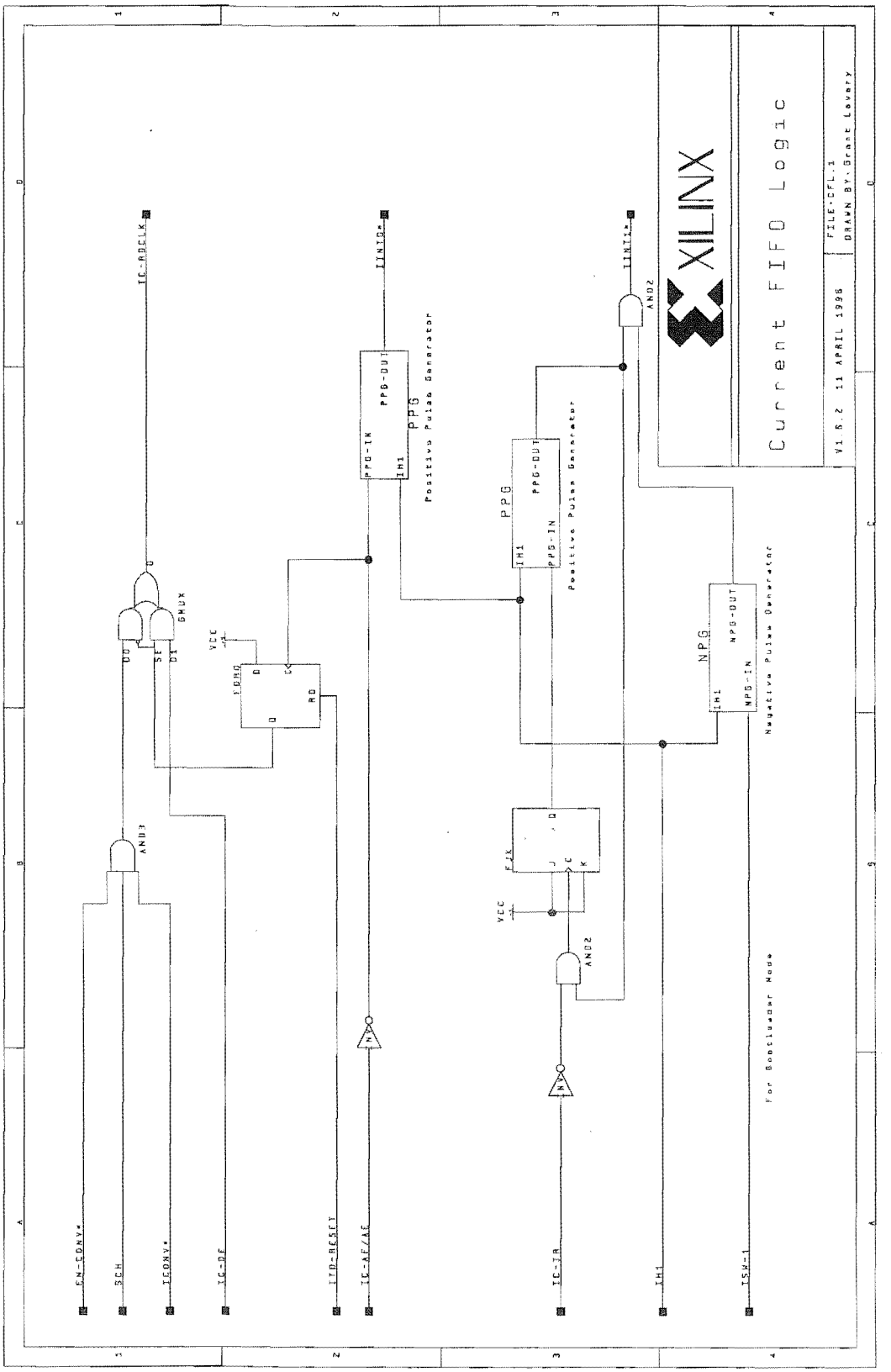


Figure J-19 Current channel FIFO logic

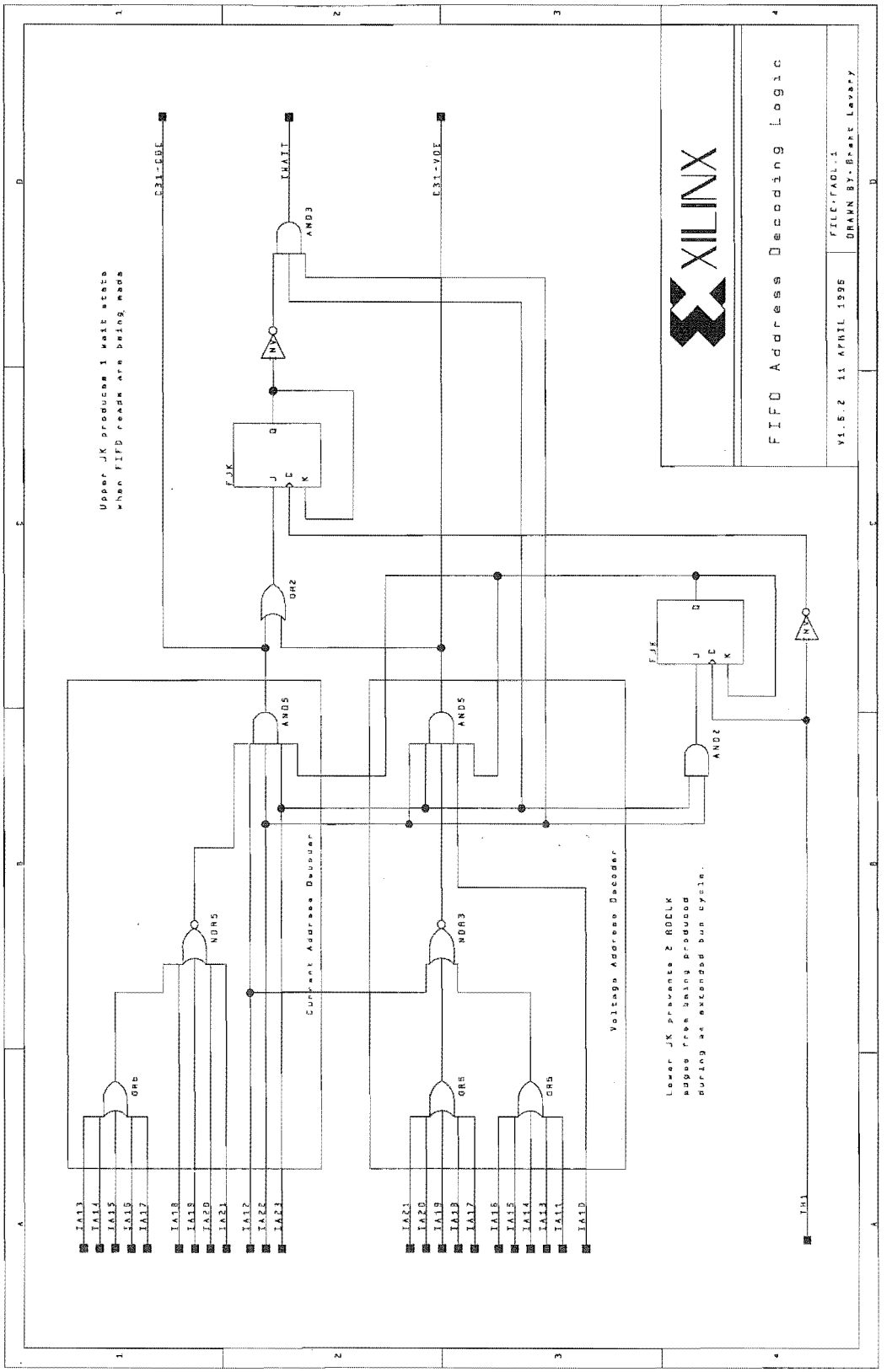


Figure J-20 FIFO address decoding logic

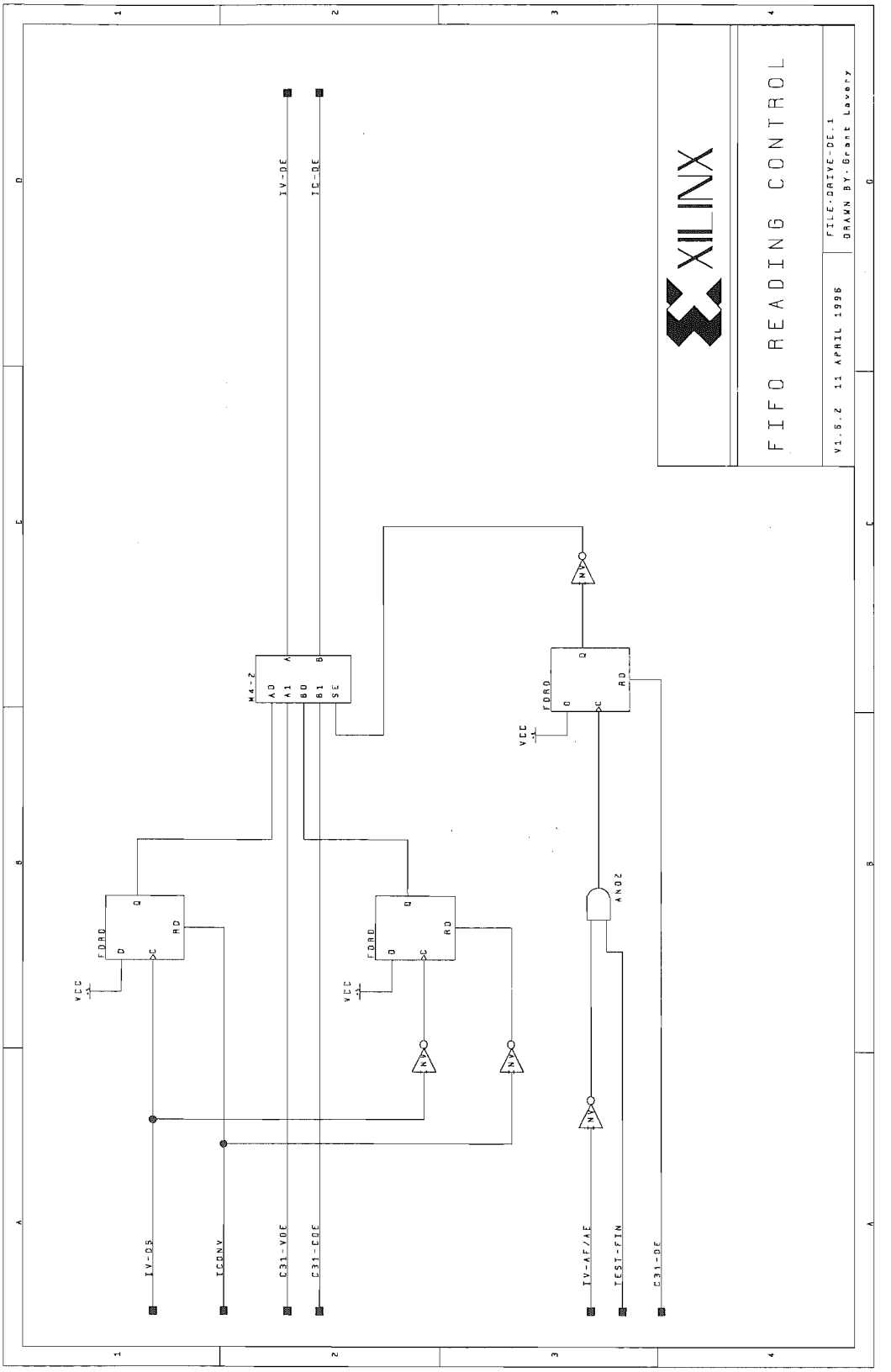


Figure J-21 FIFO output enable driving logic

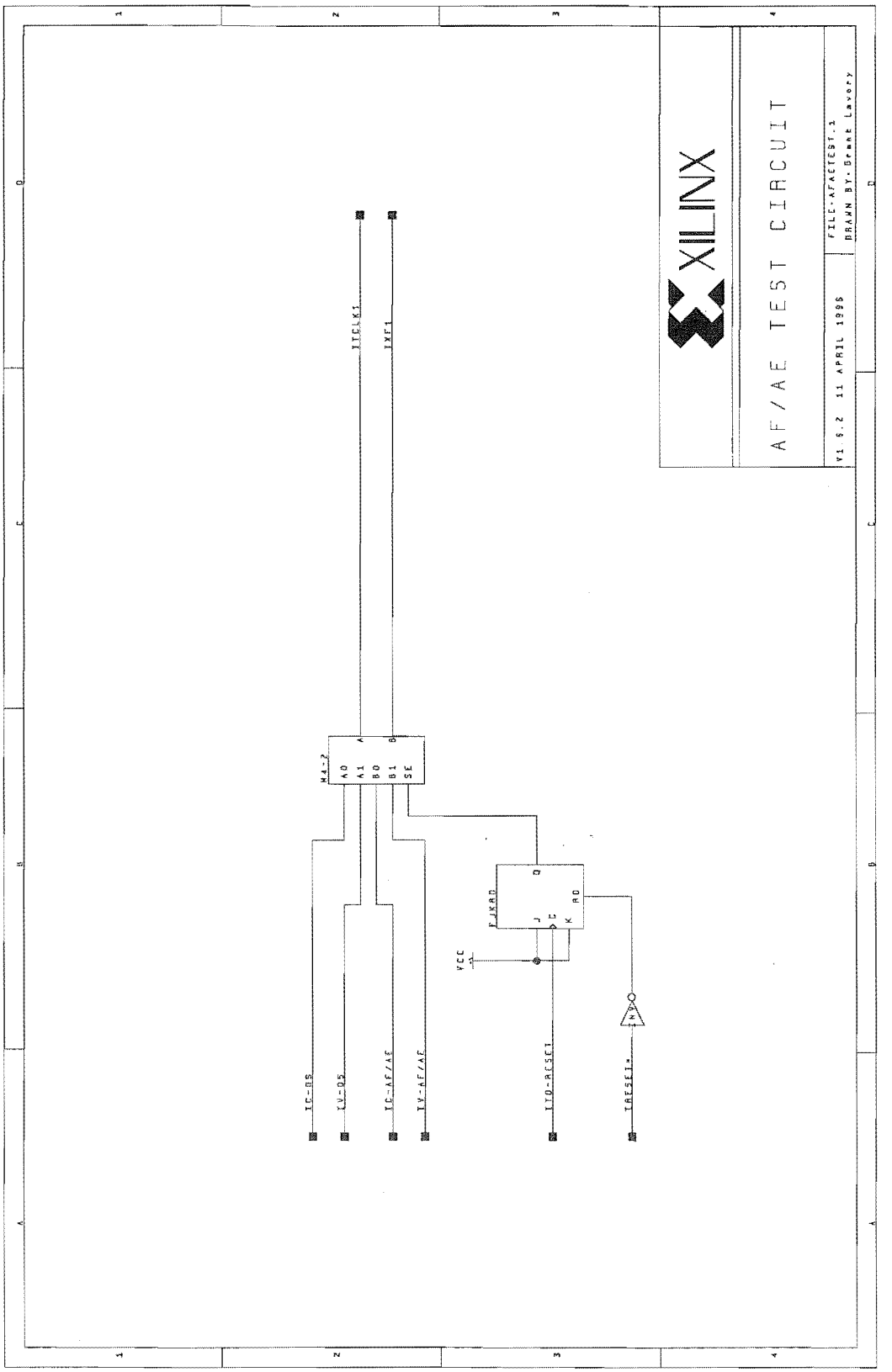


Figure J-22 FIFO AF/AE test logic

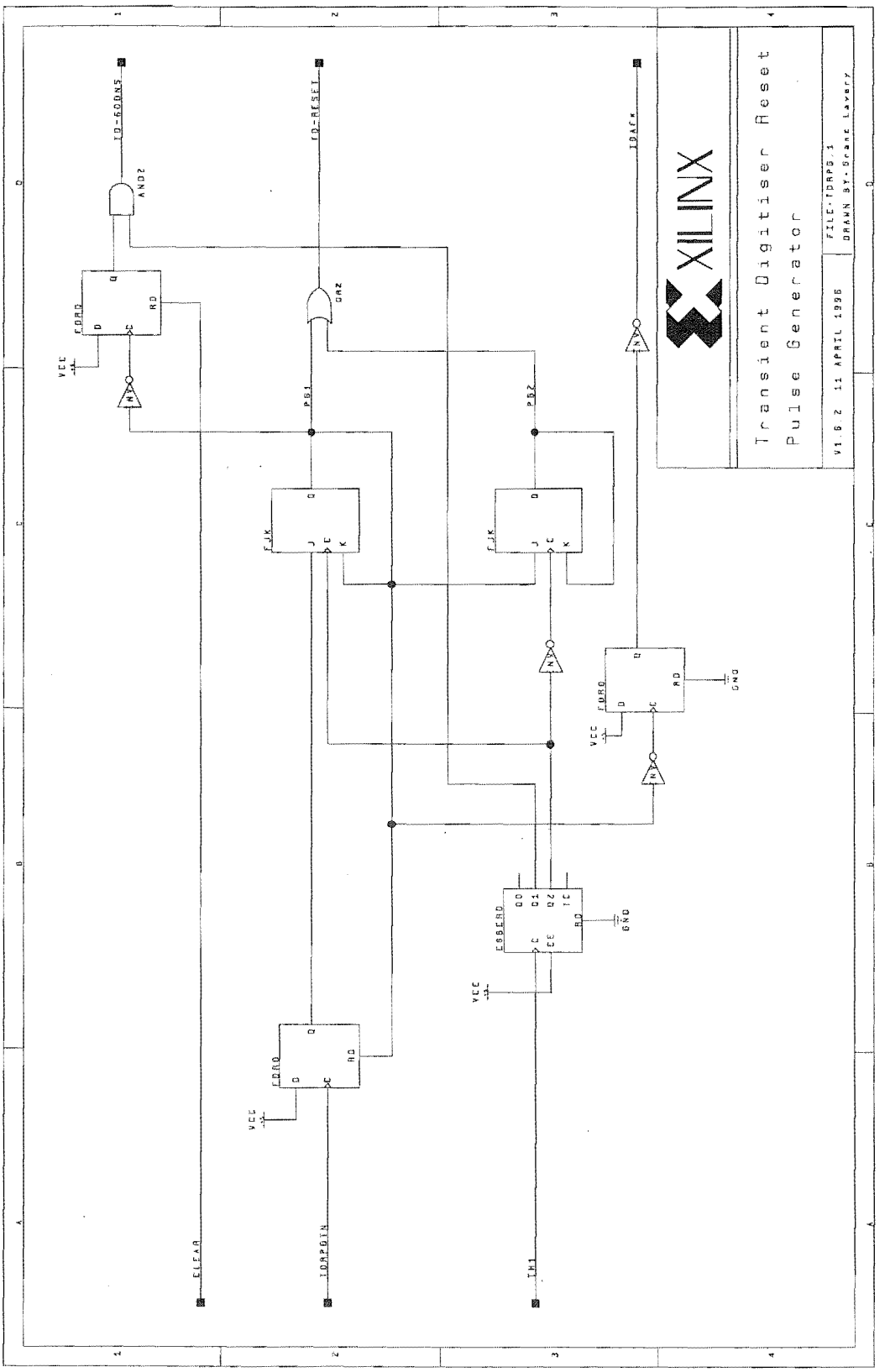


Figure J-23 TDRPG reset logic

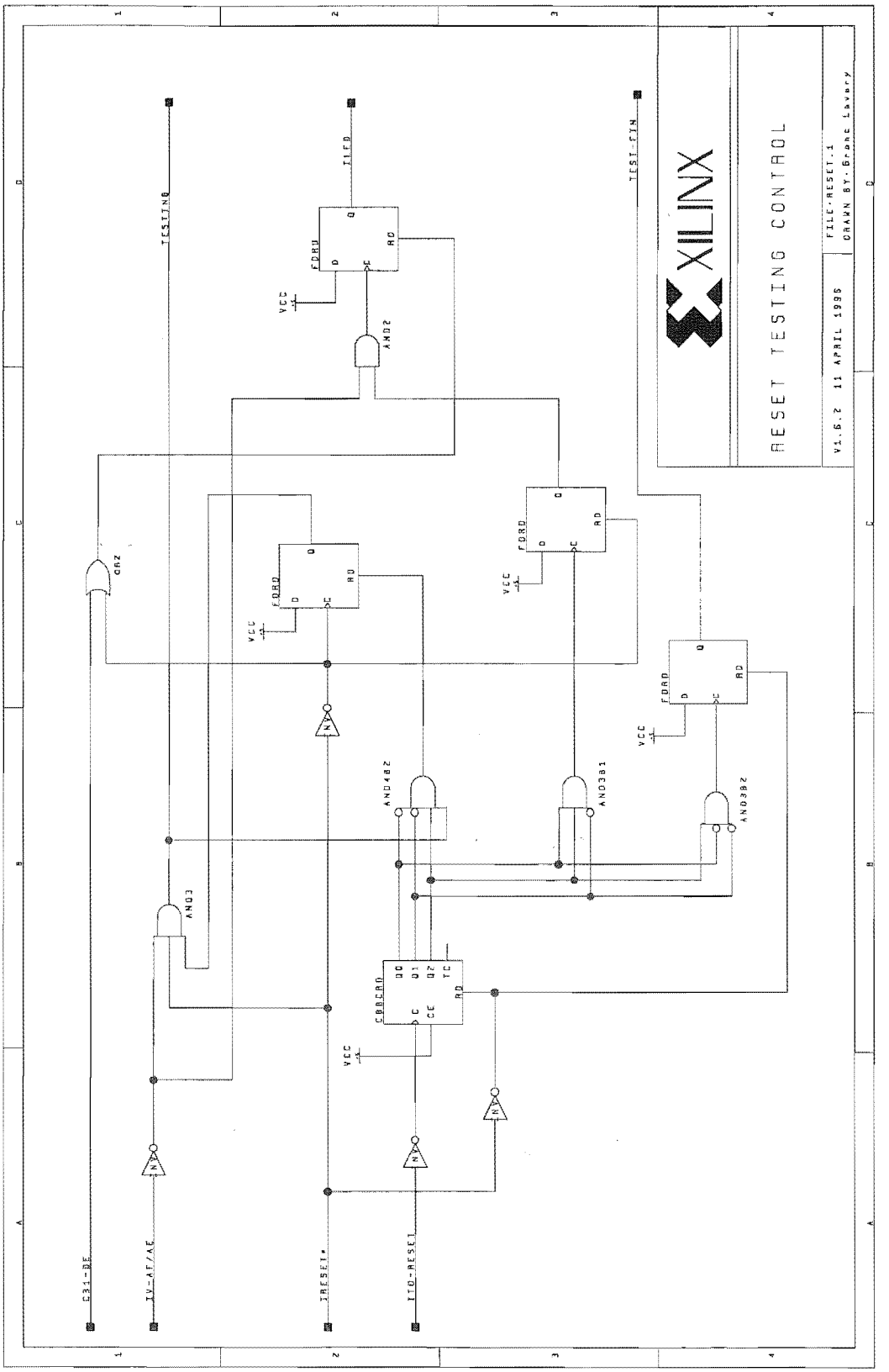


Figure J-24 Reset logic

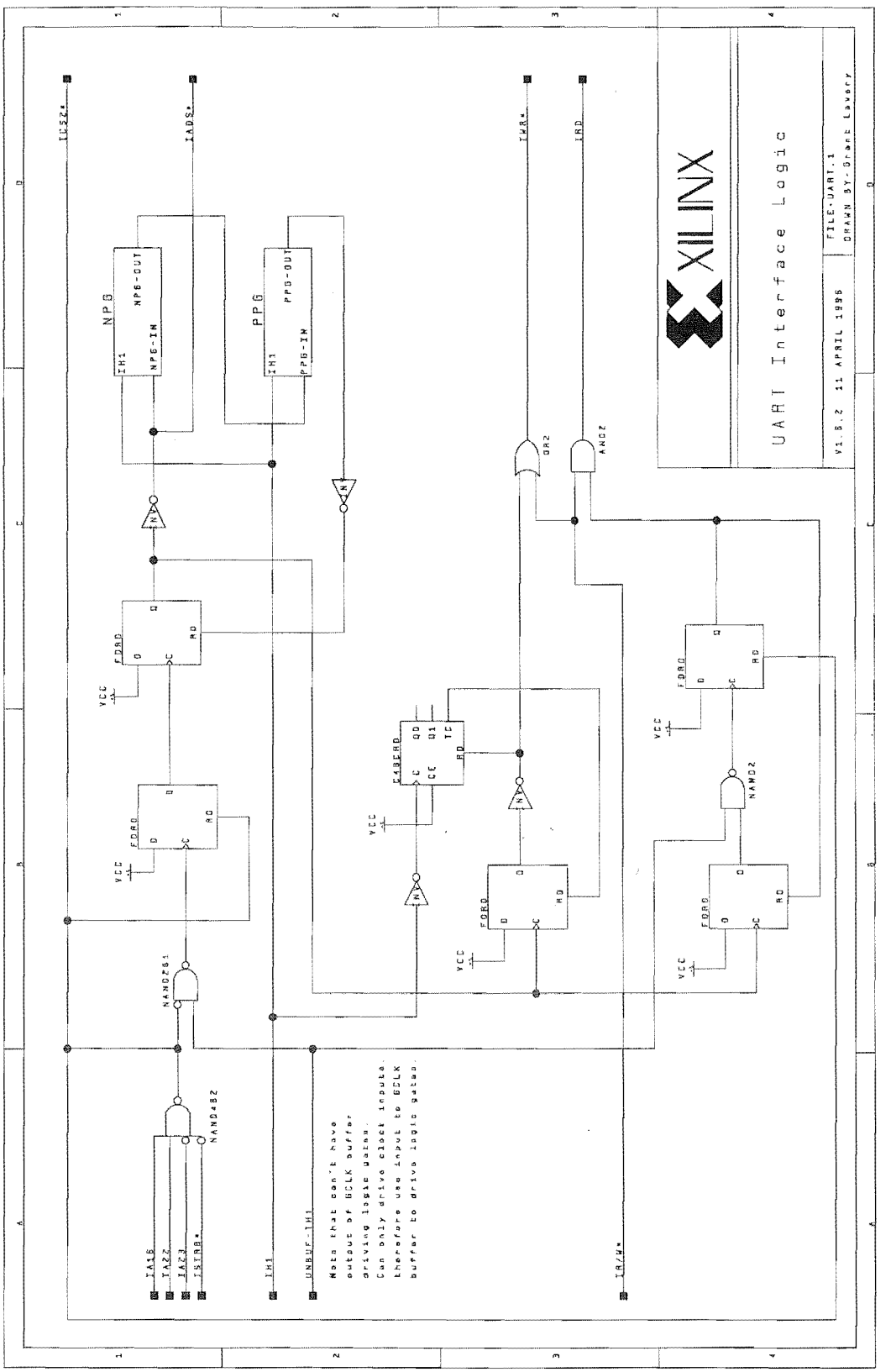


Figure J-25 UART glue logic

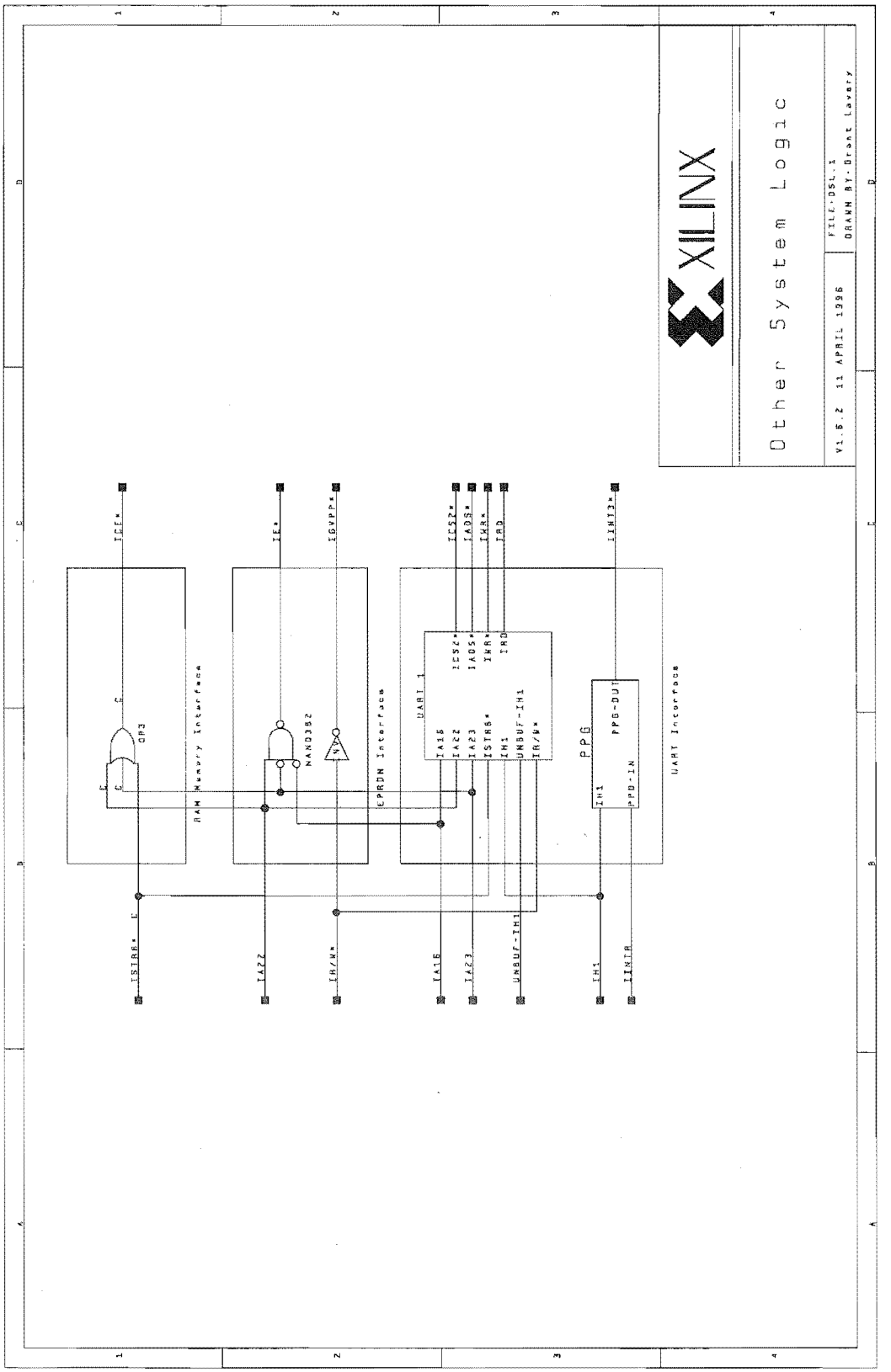


Figure J-26 Other system glue logic

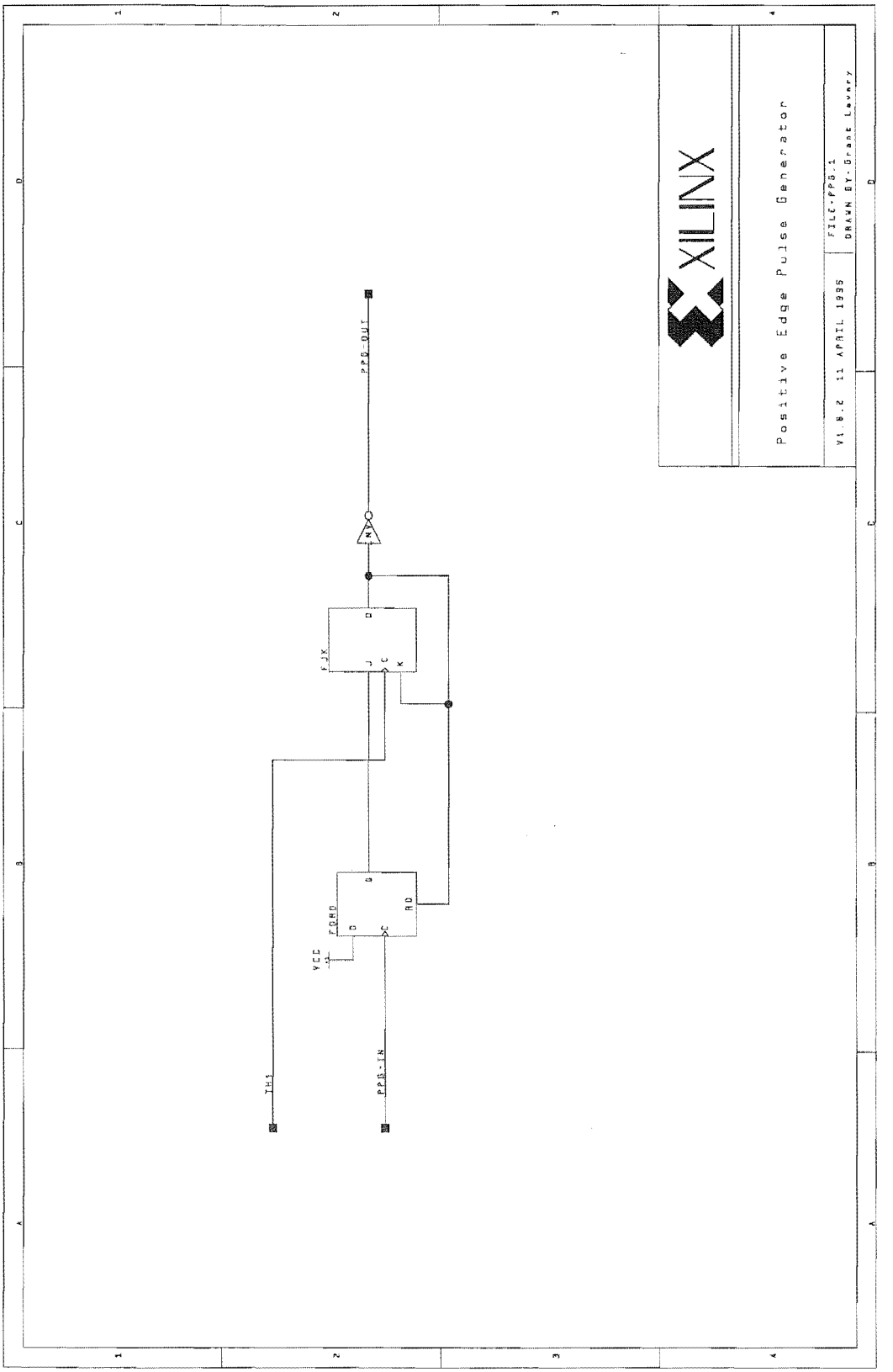


Figure J-27 Positive going edge pulse generator

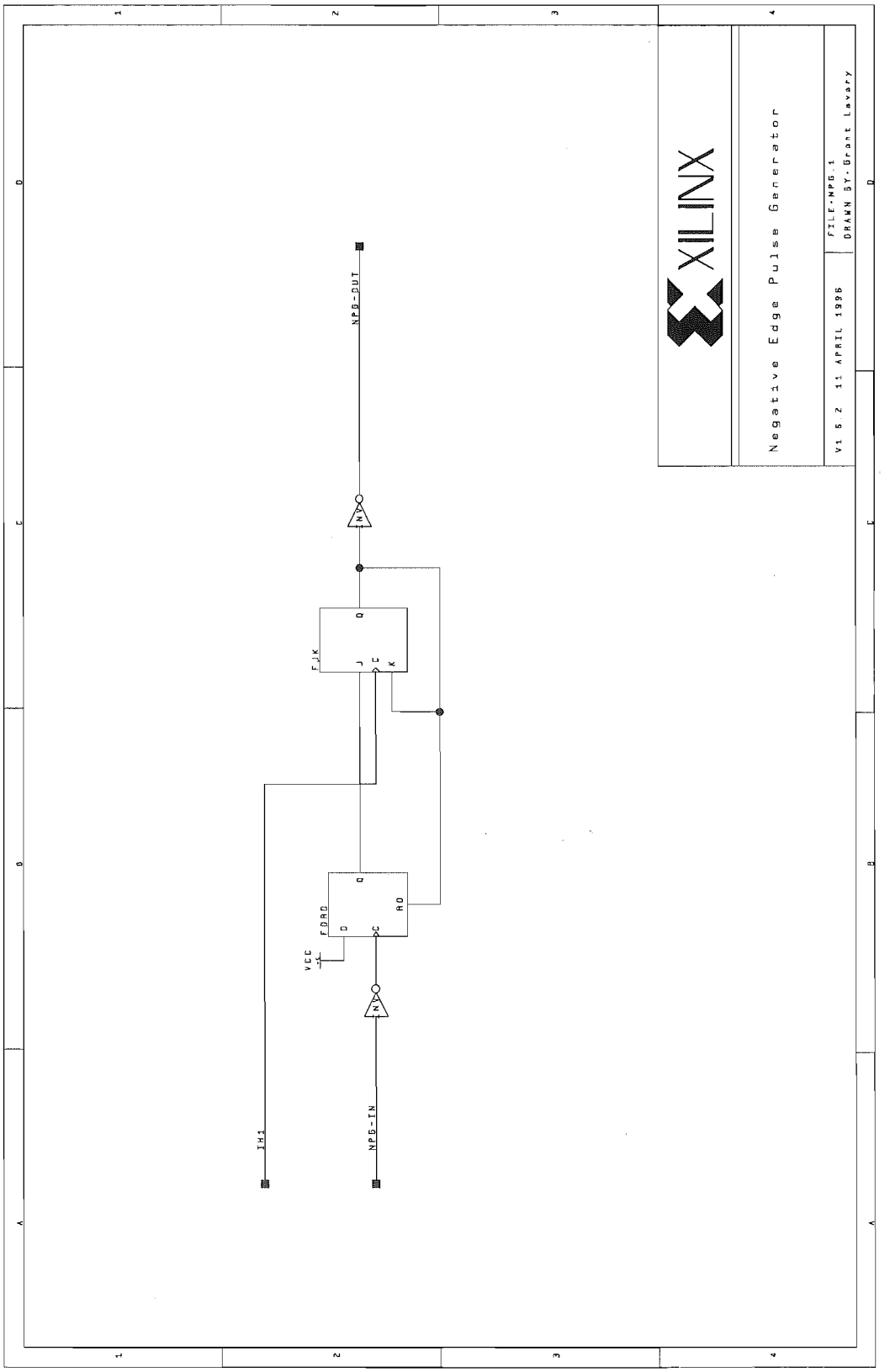


Figure J-28 Negative going edge pulse generator

Appendix K

PCB LAYOUTS

An 8 layer 220x100mm (Eurocard size) PCB was designed for the DAPM. Features of the DAPM PCB design include the following:

- A layer stack consisting of 4 signal layers, 2 ground plane layers and 2 power plane layers.
- Signal layers were shielded from each other by separating them with a ground or power plane layer.
- Data and address buses were routed first to achieve an efficient layout as they consisted of many parallel conductor tracks.
- Unused signals were routed to unused FPGA I/O pins, allowing replacement FPGA firmware to be used to reconfigure the PCB.
- Analog and digital subsystems were isolated from each other to prevent noise resulting from digital switching operations from coupling into the analog subsystem. Analog and digital circuitry were powered from separate voltage regulators.

Layout artwork follows for the DAPM, IGM, and the sampling clock generator modification.

K.1 DAPM

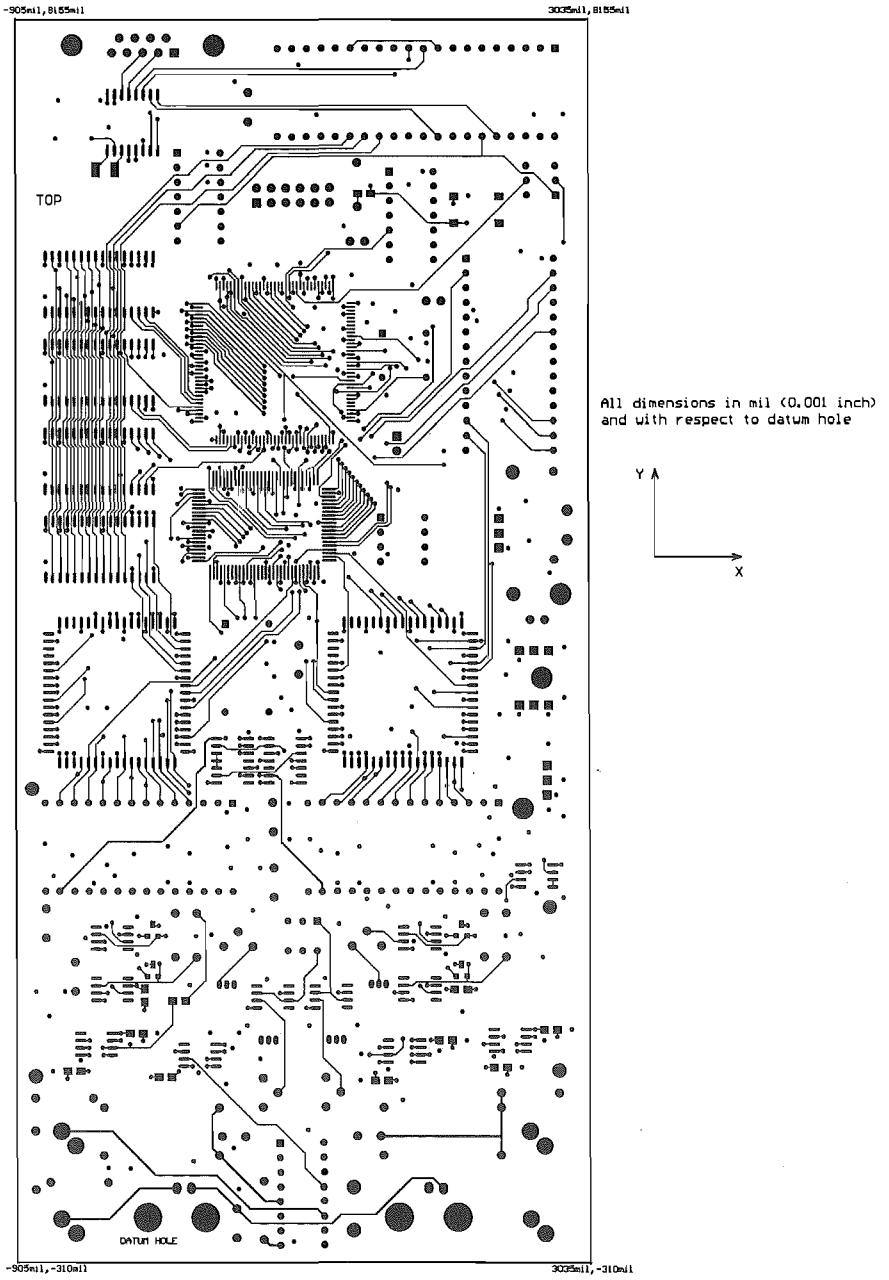


Figure K-1 Top signal layer (76% of full scale)

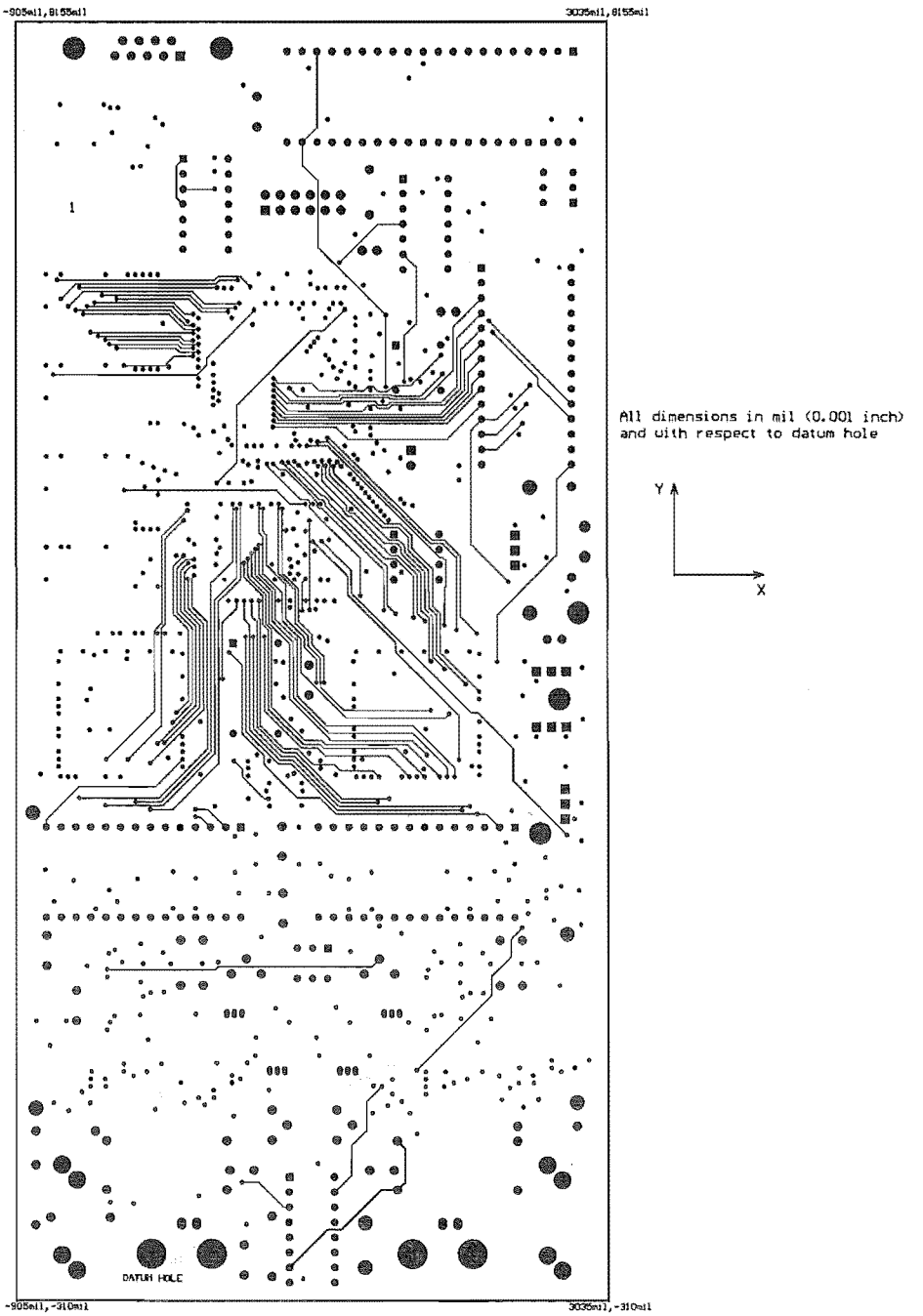


Figure K-2 Mid signal layer 1 (80% full size)

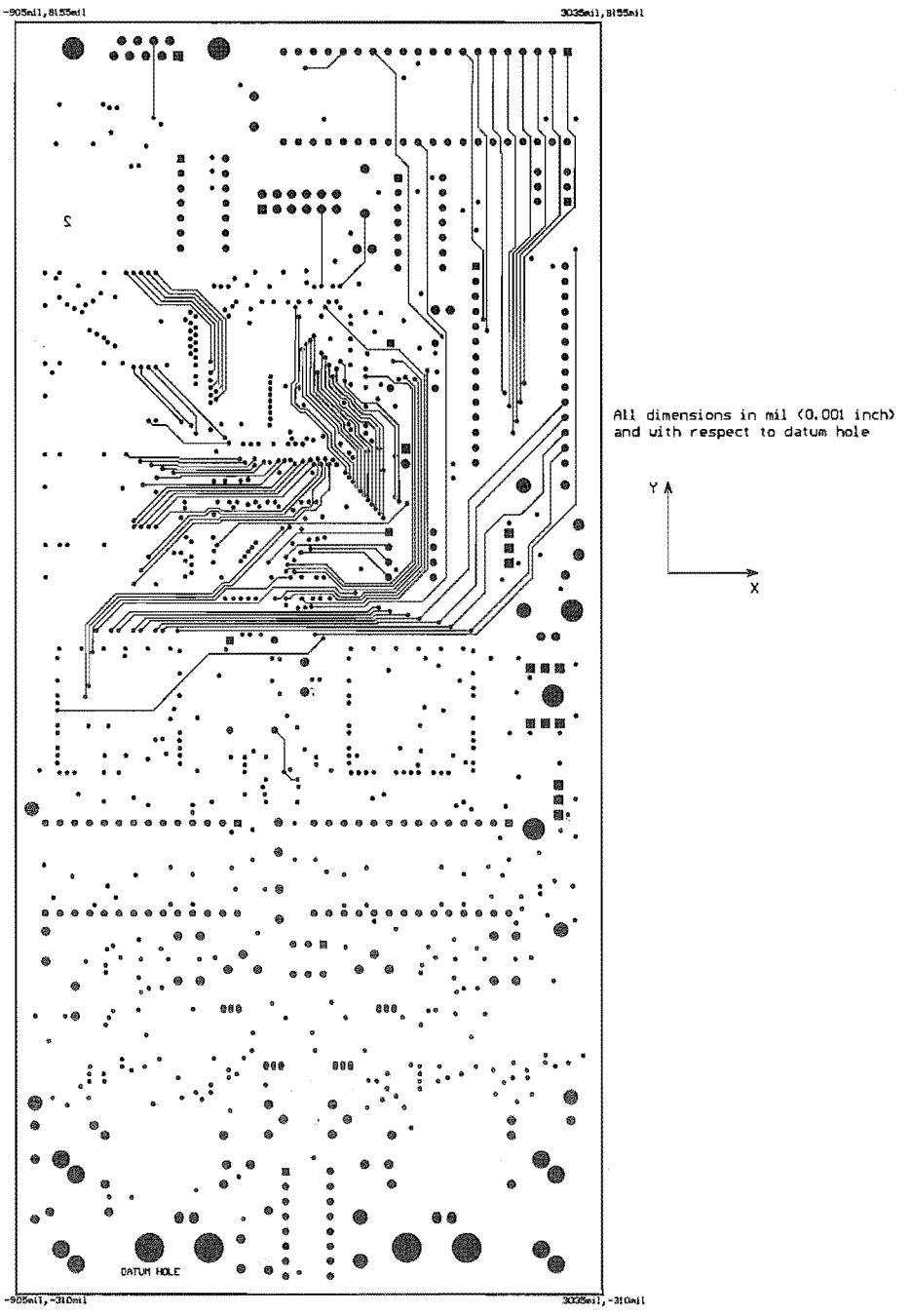


Figure K-3 Mid signal layer 2

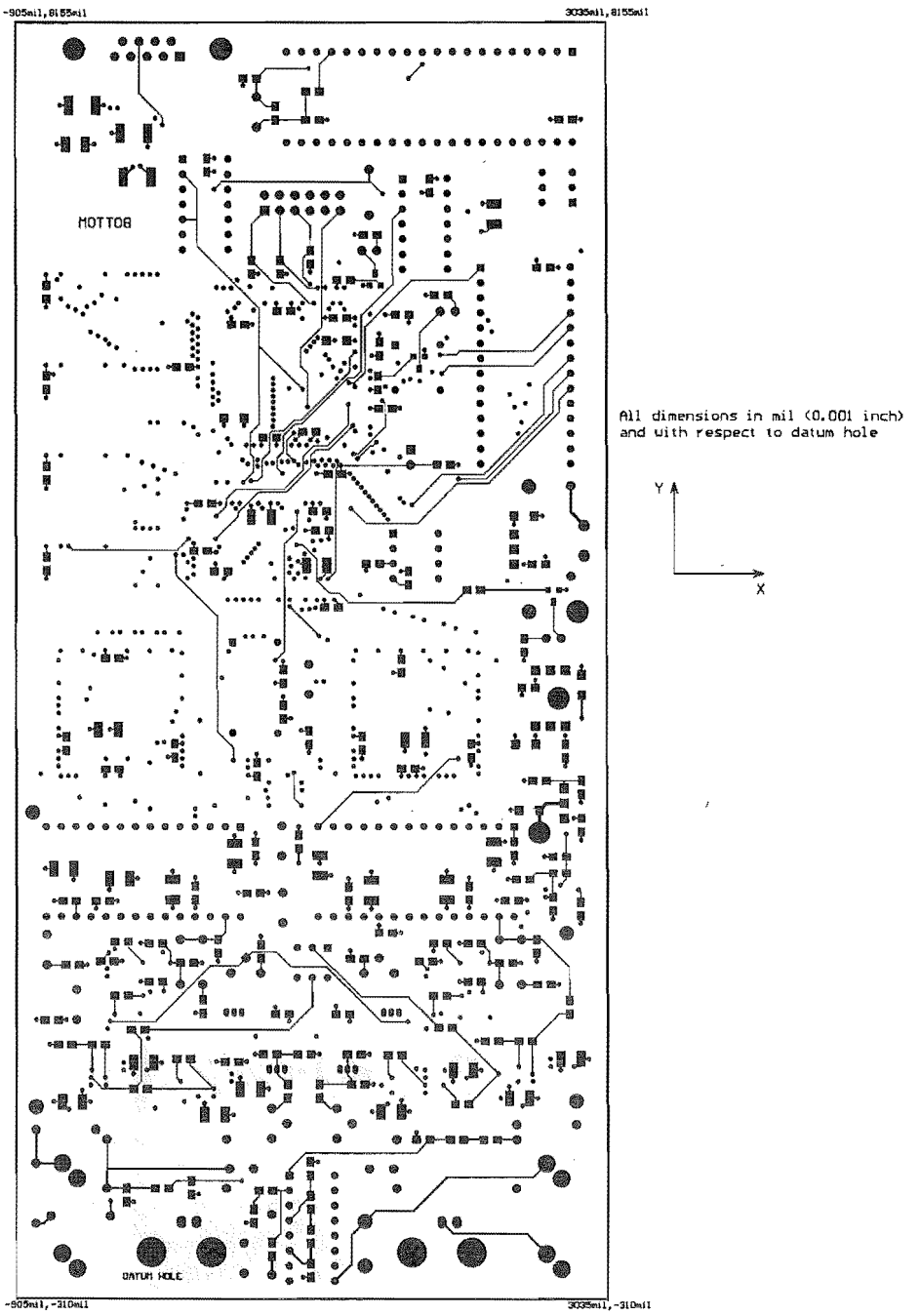


Figure K-4 Bottom signal layer

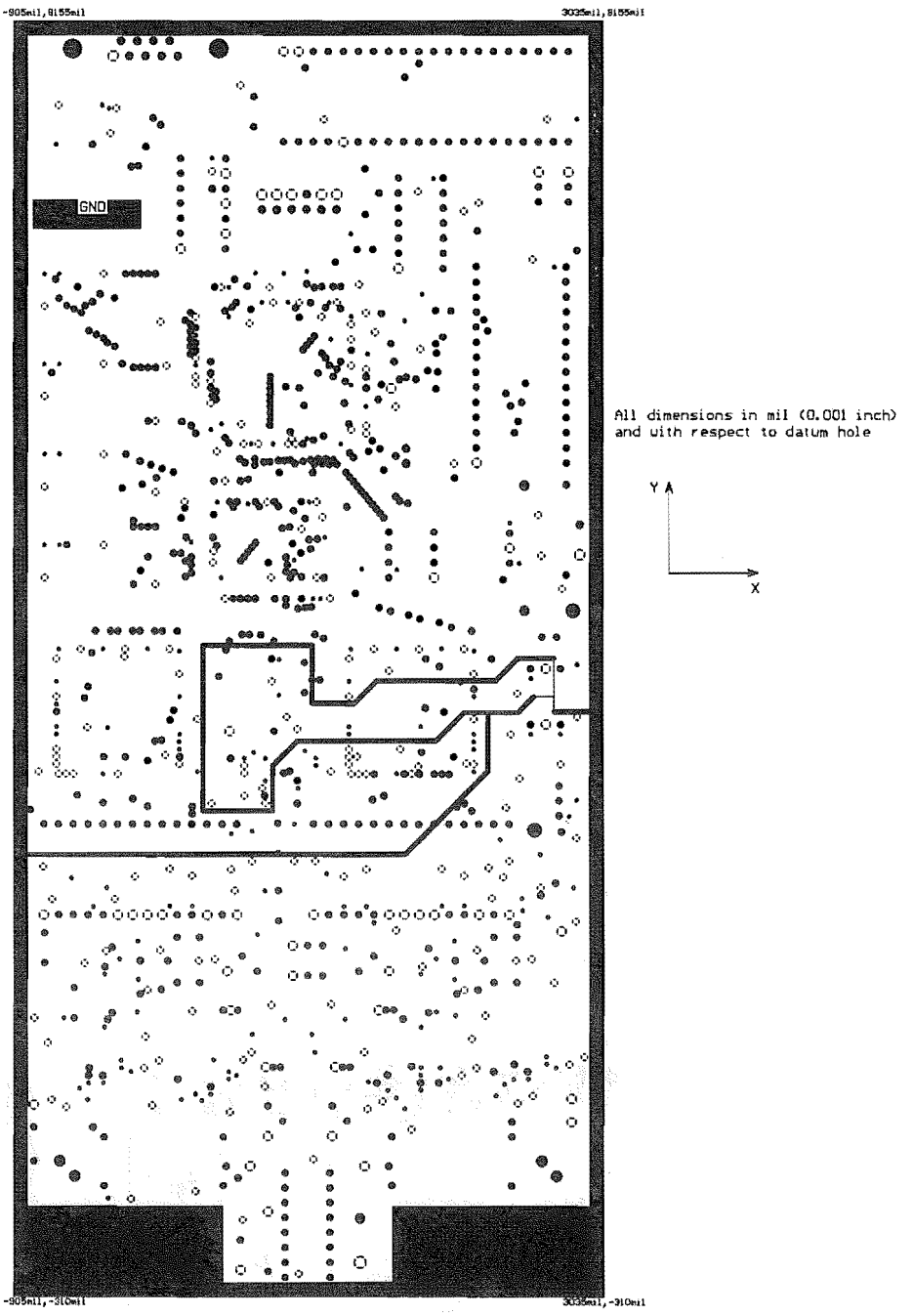


Figure K-5 Analog and digital ground planes (printed inverted)

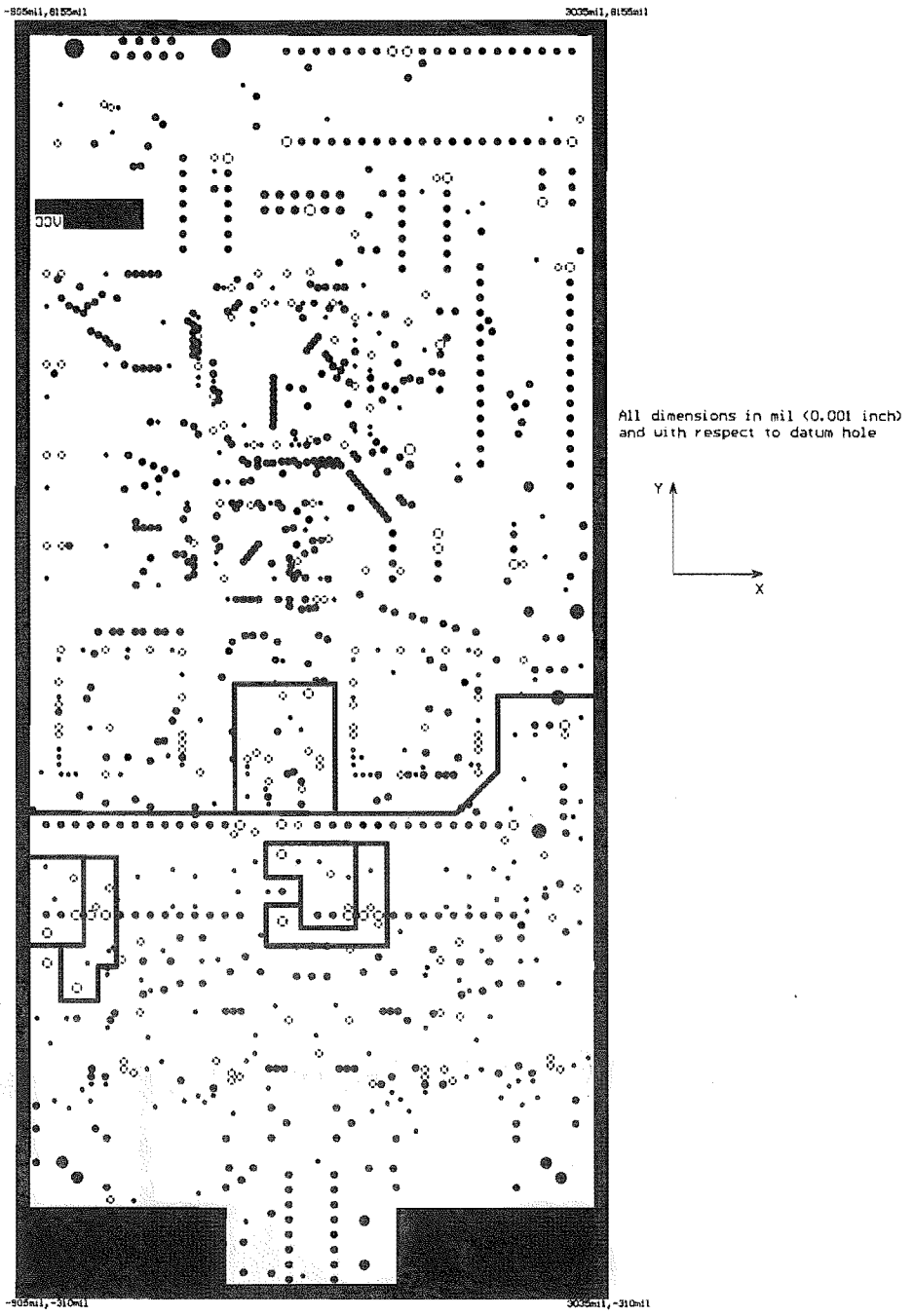


Figure K-6 Analog, digital, and sampling clock generator +5V power supply planes (inverted)

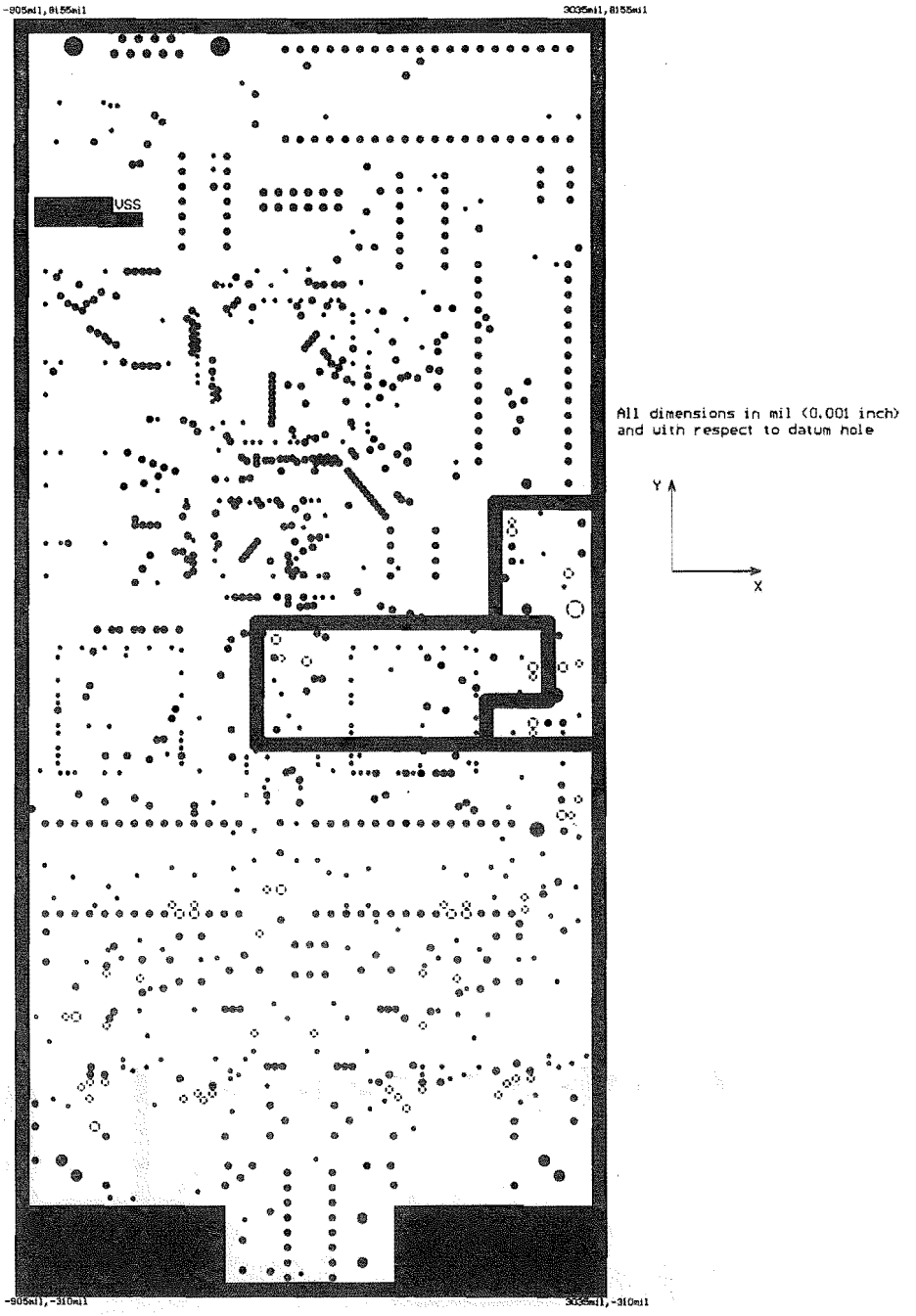


Figure K-7 Analog –5.2V power plane (inverted)

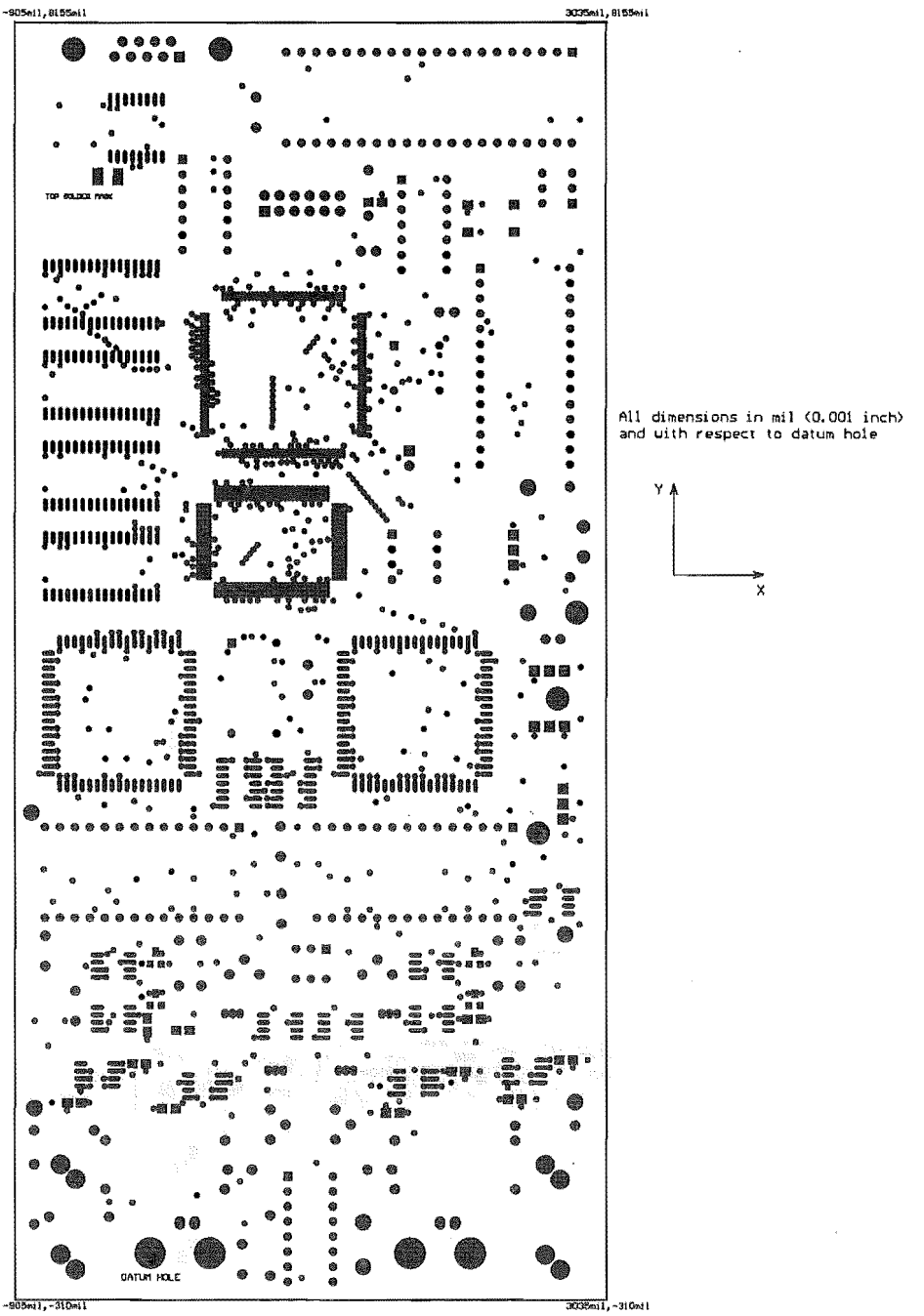


Figure K-8 Top solder layer

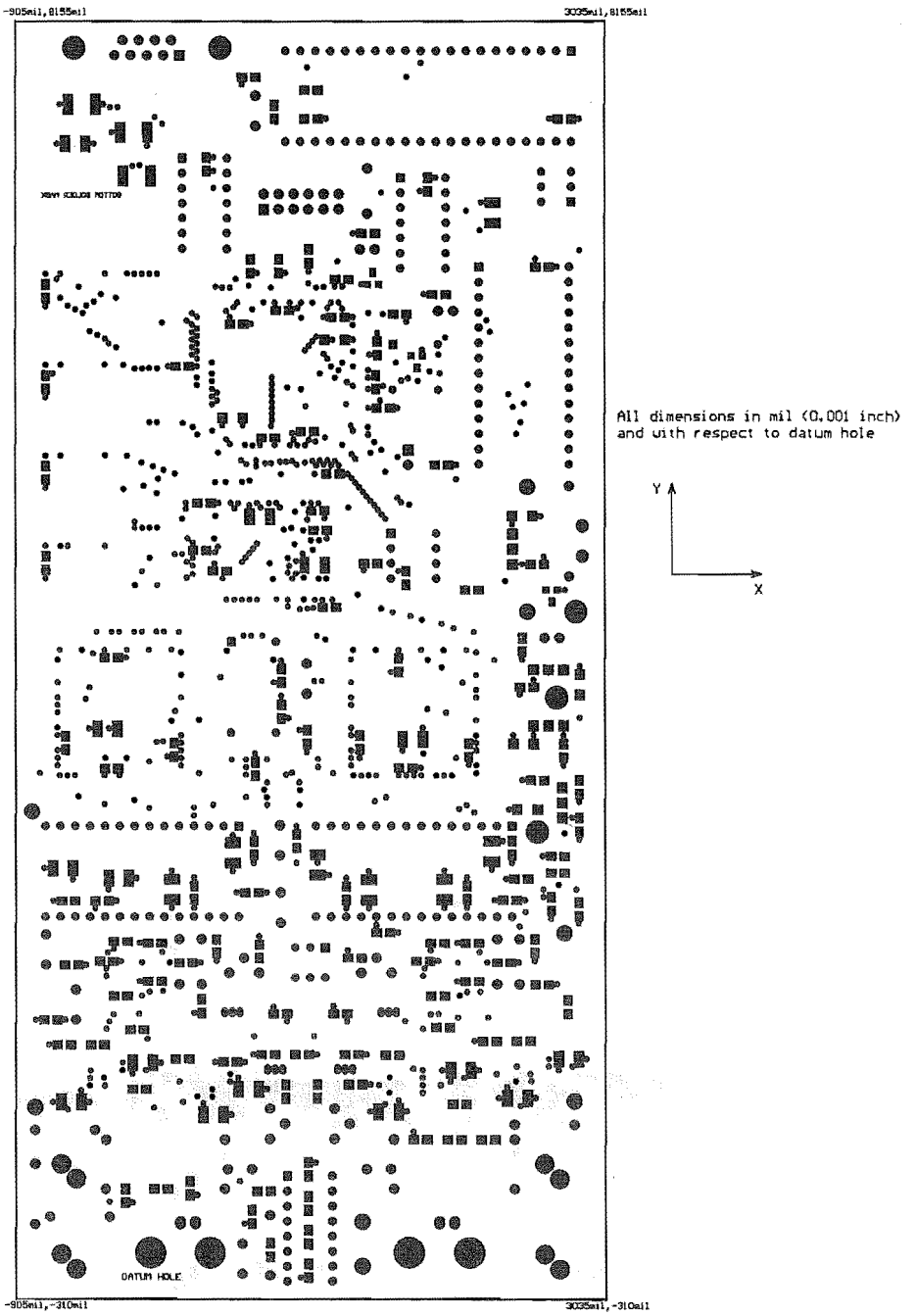


Figure K-9 Bottom solder layer

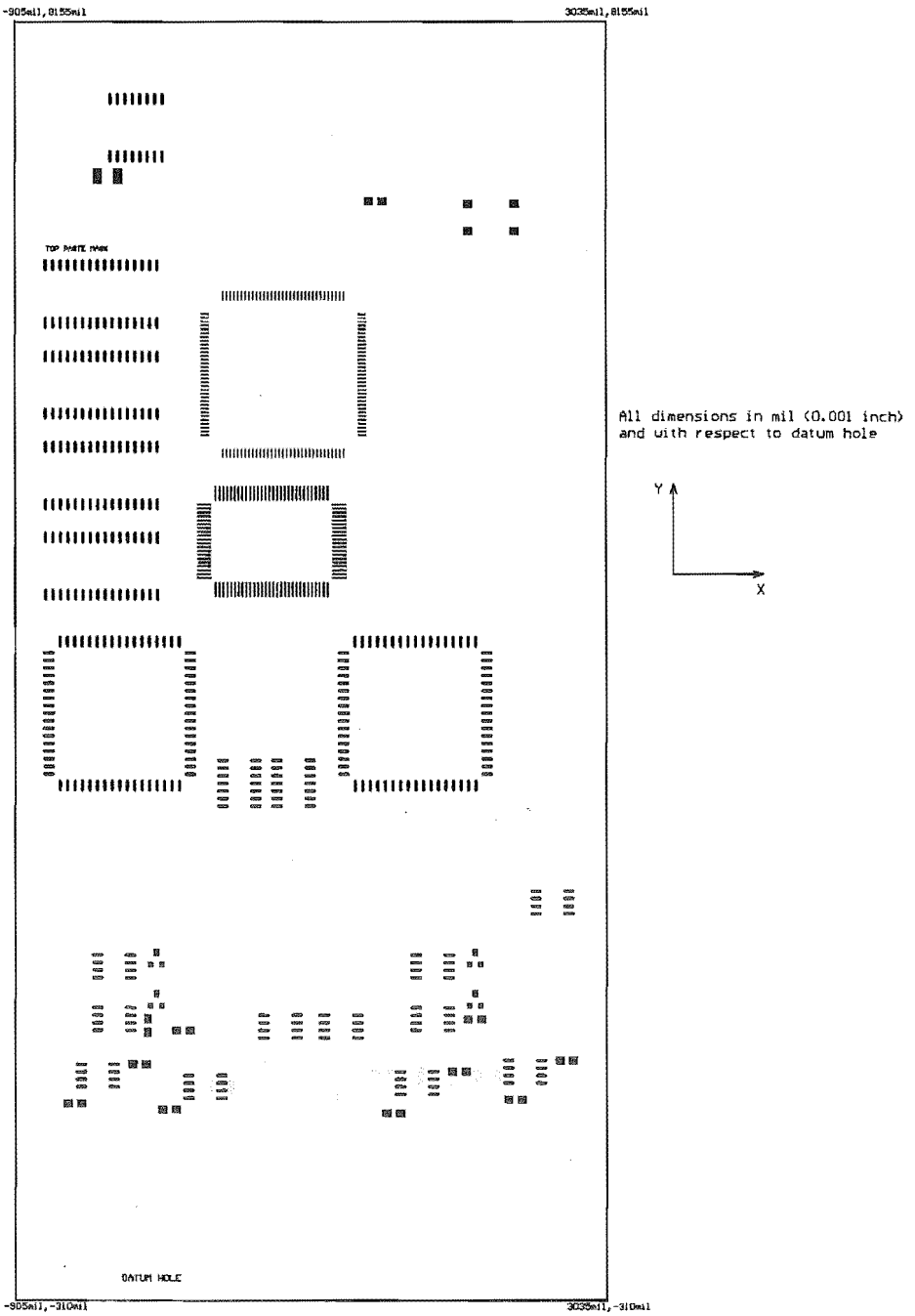


Figure K-10 Top solder paste layer

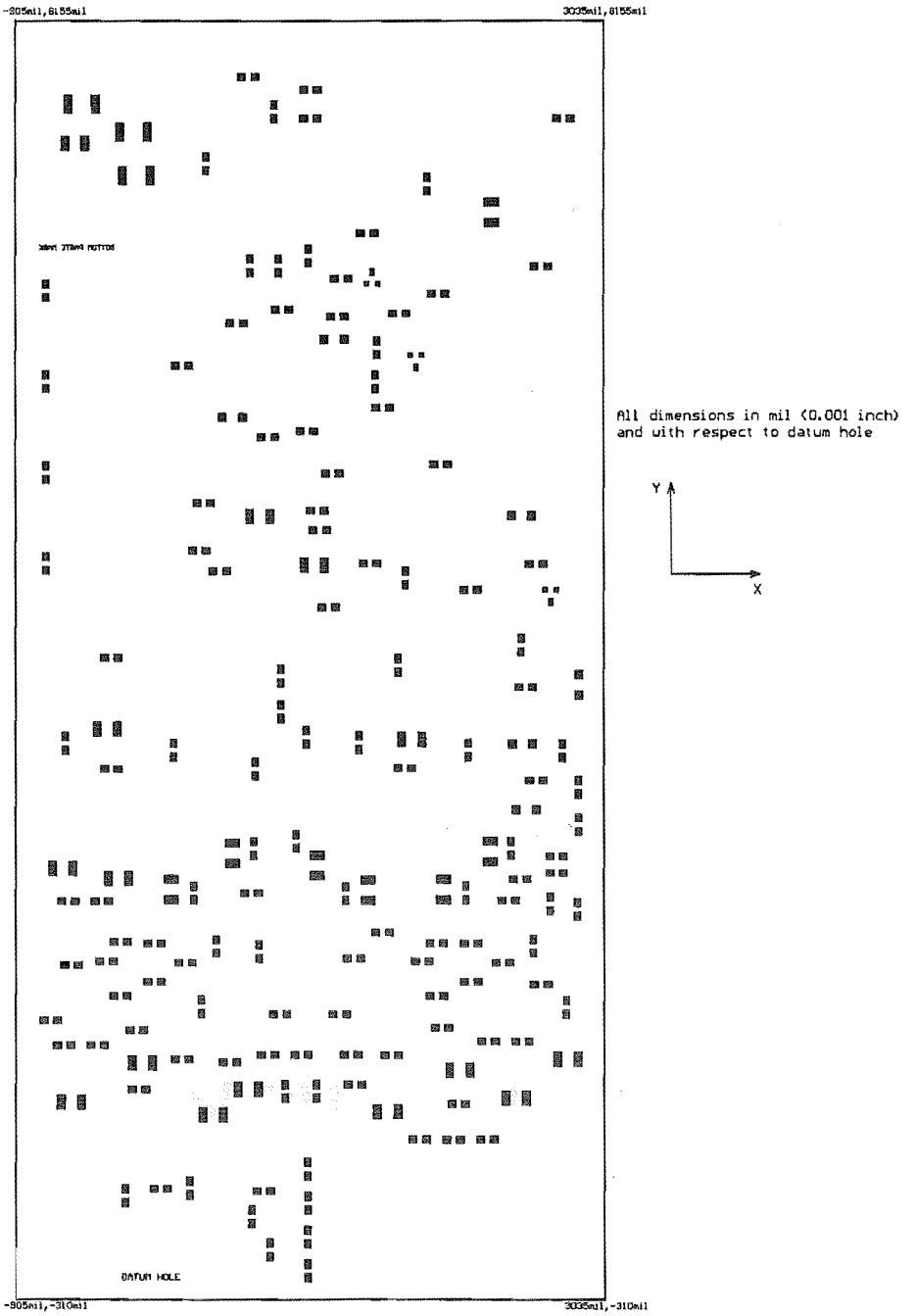


Figure K-11 Bottom solder paste layer

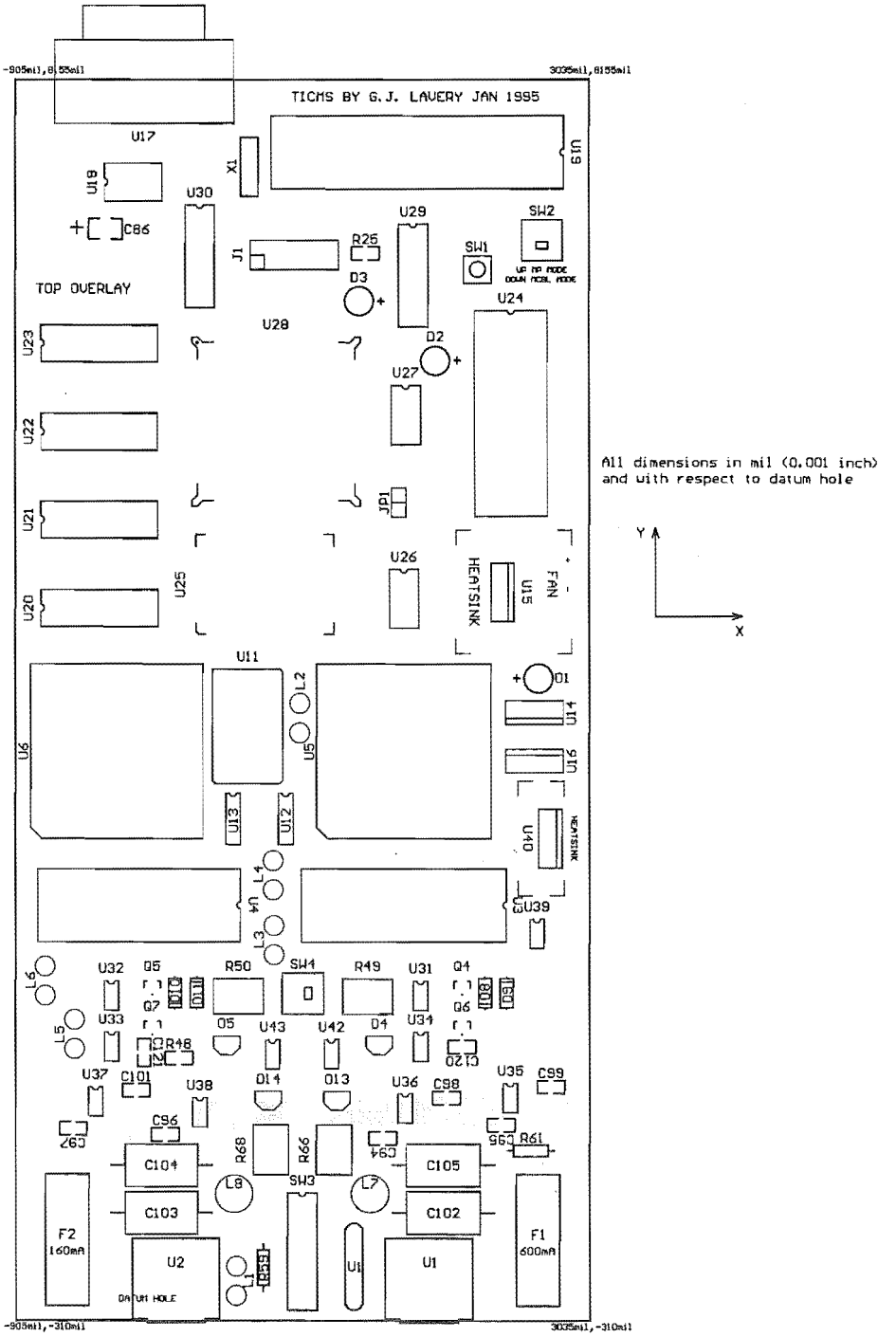


Figure K-12 Top silk screen layer

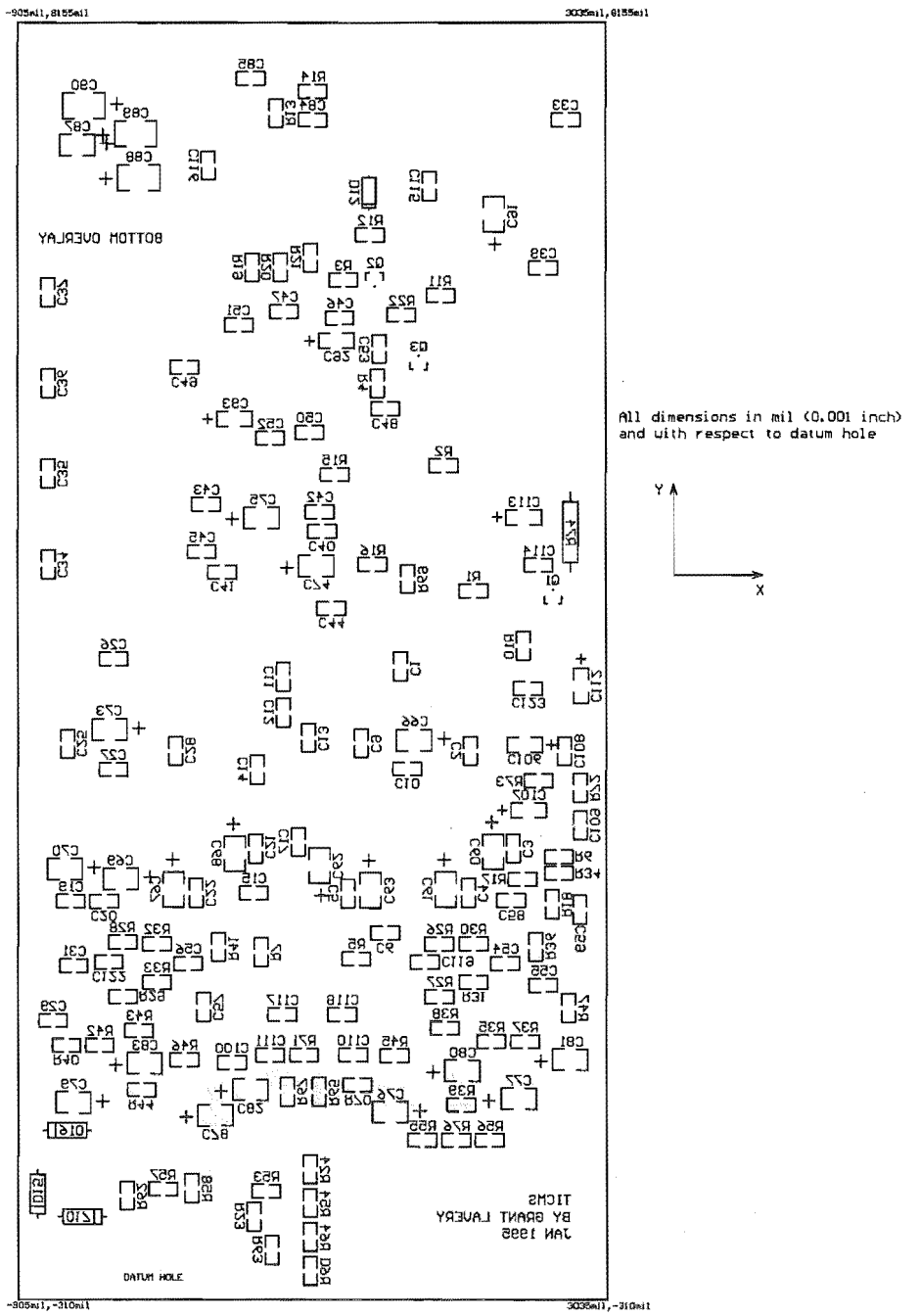


Figure K-13 Bottom silk screen layer

K.2 IGM

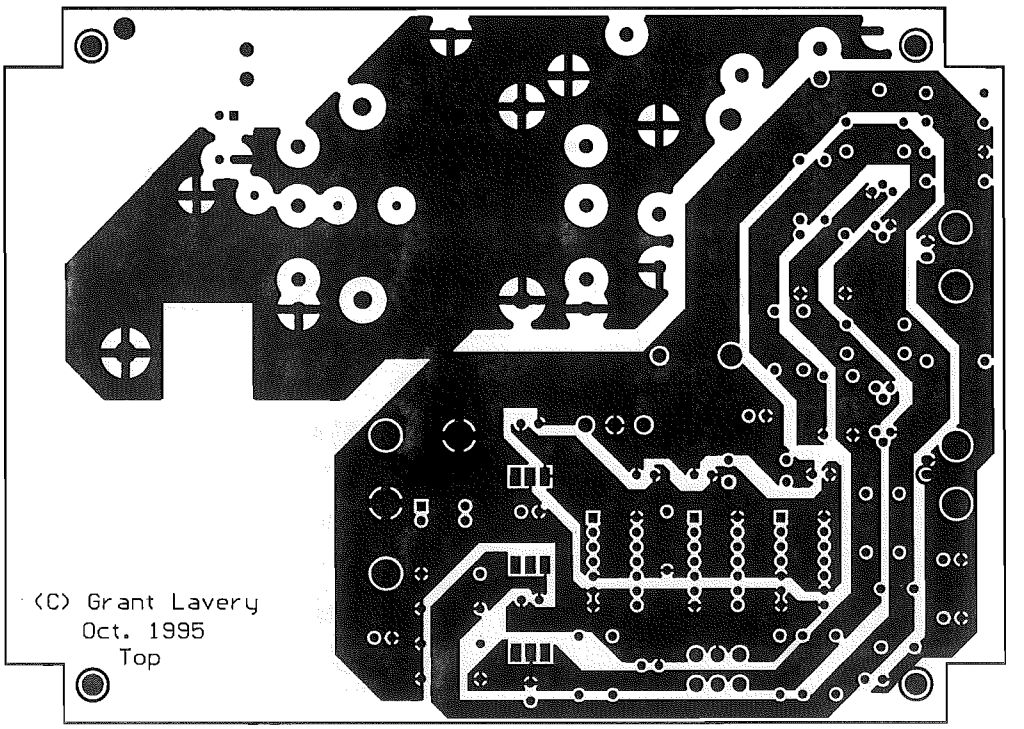


Figure K-14 Top signal layer (76% full size)

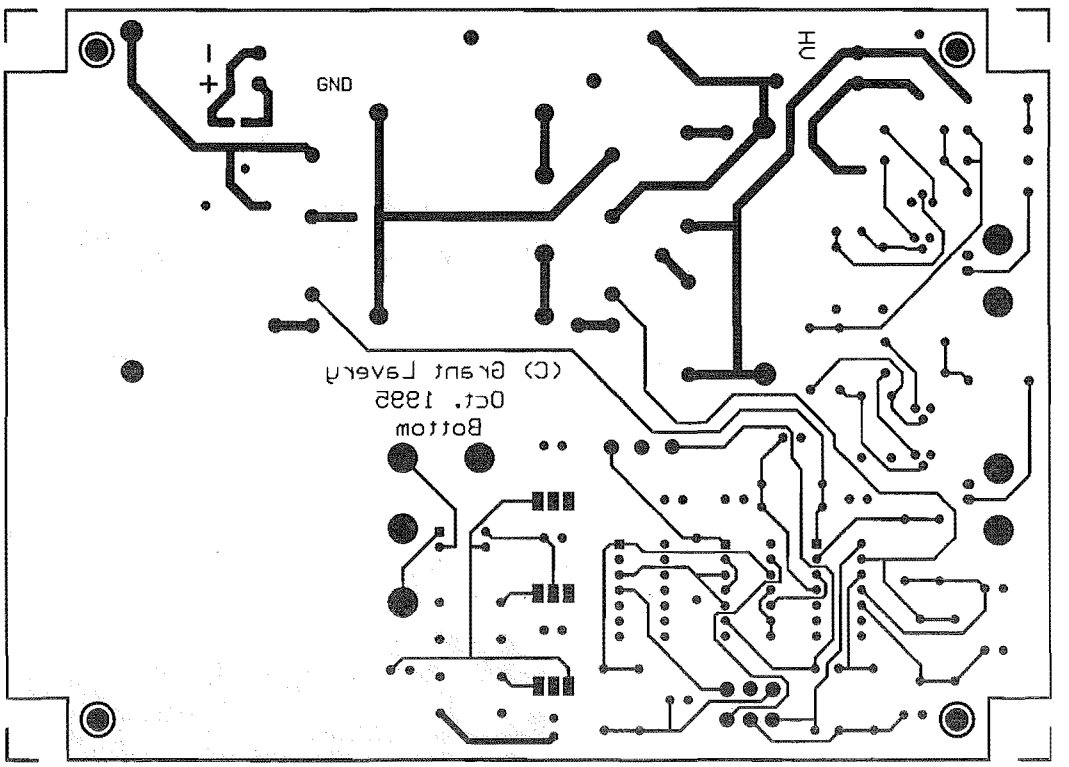


Figure K-15 Bottom signal layer (80% full size)

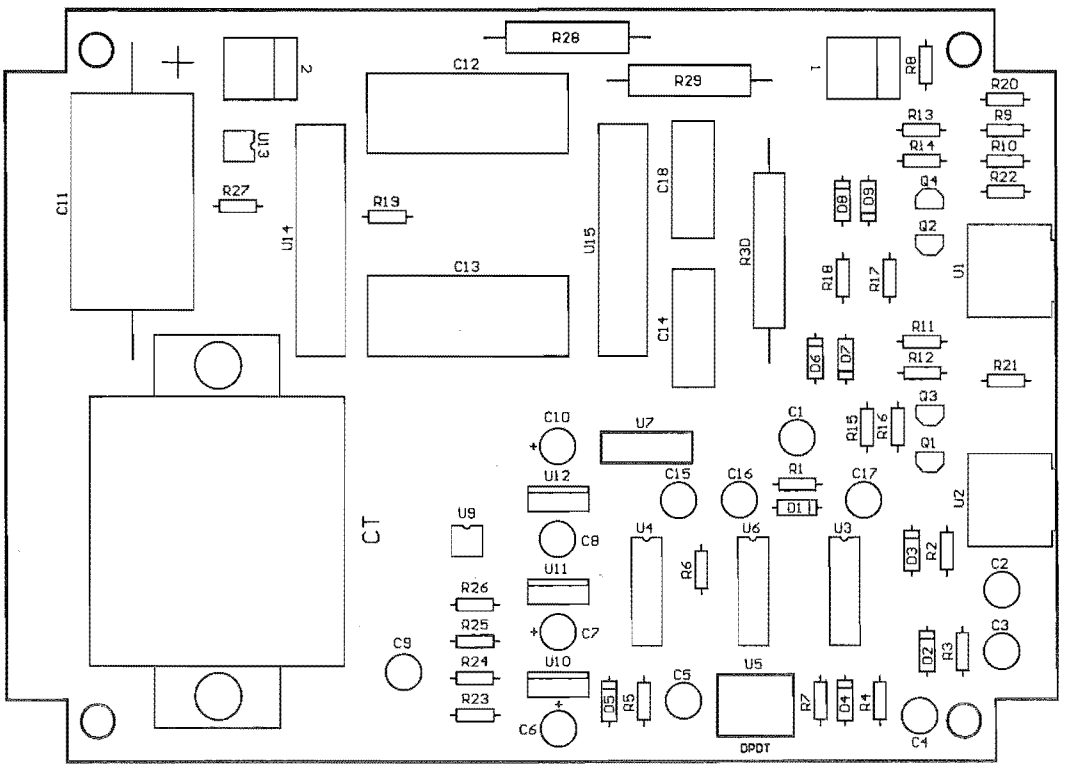


Figure K-16 Top silk screen layer

K.3 Sampling Clock Generator Modification

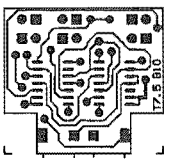


Figure K-17 Top signal layer (76% full size)

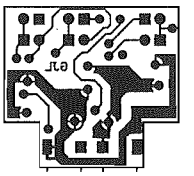


Figure K-18 Bottom signal layer (80% full size)

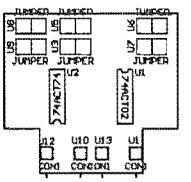


Figure K-19 Top silk screen layer